

Compal Confidential

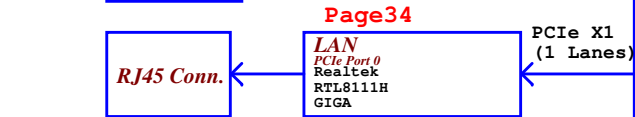
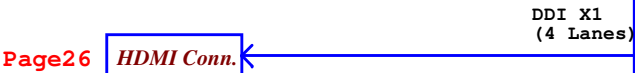
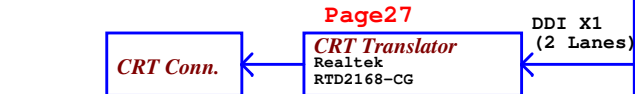
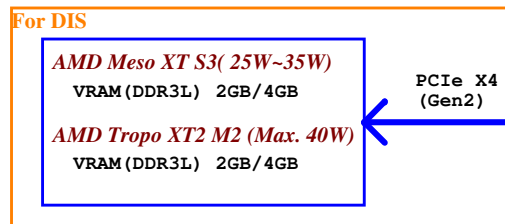
AIWZ0/AIWZ1
DIS M/B Schematics Document
Intel Boardwell U Processor with DDR3L
AMD Meso XT / Tropo XT2

2015-02-02

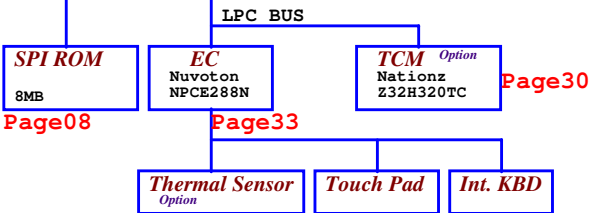
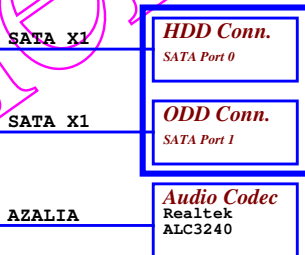
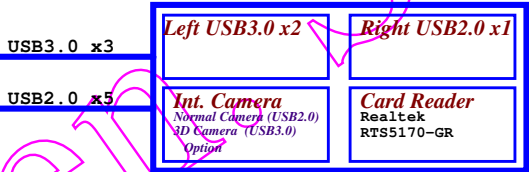
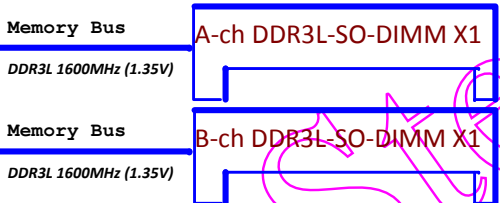
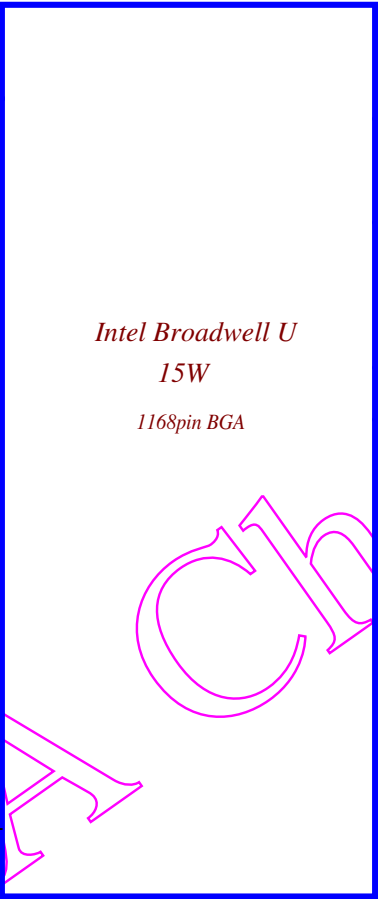
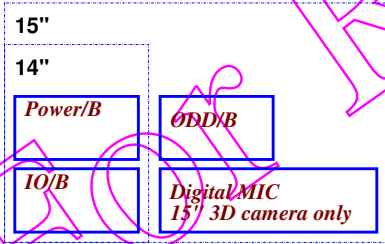
LA-C281P

REV : 1.0

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Sub-borad



Power plane

State	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +VCC_CORE +VGA_CORE +1.8VS +0.675VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011x	Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	Device	Address
DDR_JDIMM1	1010 000x A0h	Internal thermal sensor	0100 0001 41h
DDR_JDIMM2	1010 010x A4h		

SMBUS Control Table

	SOURCE	CRT	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
EC_SMB_CK1	NPCE288	✗	✓	✗	✗	✗	✗	✗
EC_SMB_DA1	+3VALW		+3VALW					
EC_SMB_CK2	NPCE288	✓	✗	✗	✗	✗	✓	✓
EC_SMB_DA2	+3VS	+3VS					+3VS	+3VALW
PCH_SMB_CLK	PCH	✗	✗	✗	✓	✗	✗	✗
PCH_SMB_DATA	+3VALW				+3VS			
PCH_SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗
PCH_SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✗	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS		✓			+3VGS	

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)USB3.0
		1	USB Port (Left Side)USB3.0
	UHCI1	2	Sub Board
		3	CardReader
	UHCI2	4	Touch Screen
		5	Camera
EHCI1	UHCI3	6	Bluetooth (NGFF)
		7	
	UHCI4	8	
		9	
	UHCI5	10	
		11	
EHCI1	UHCI6	12	
		13	

BDW_CPU

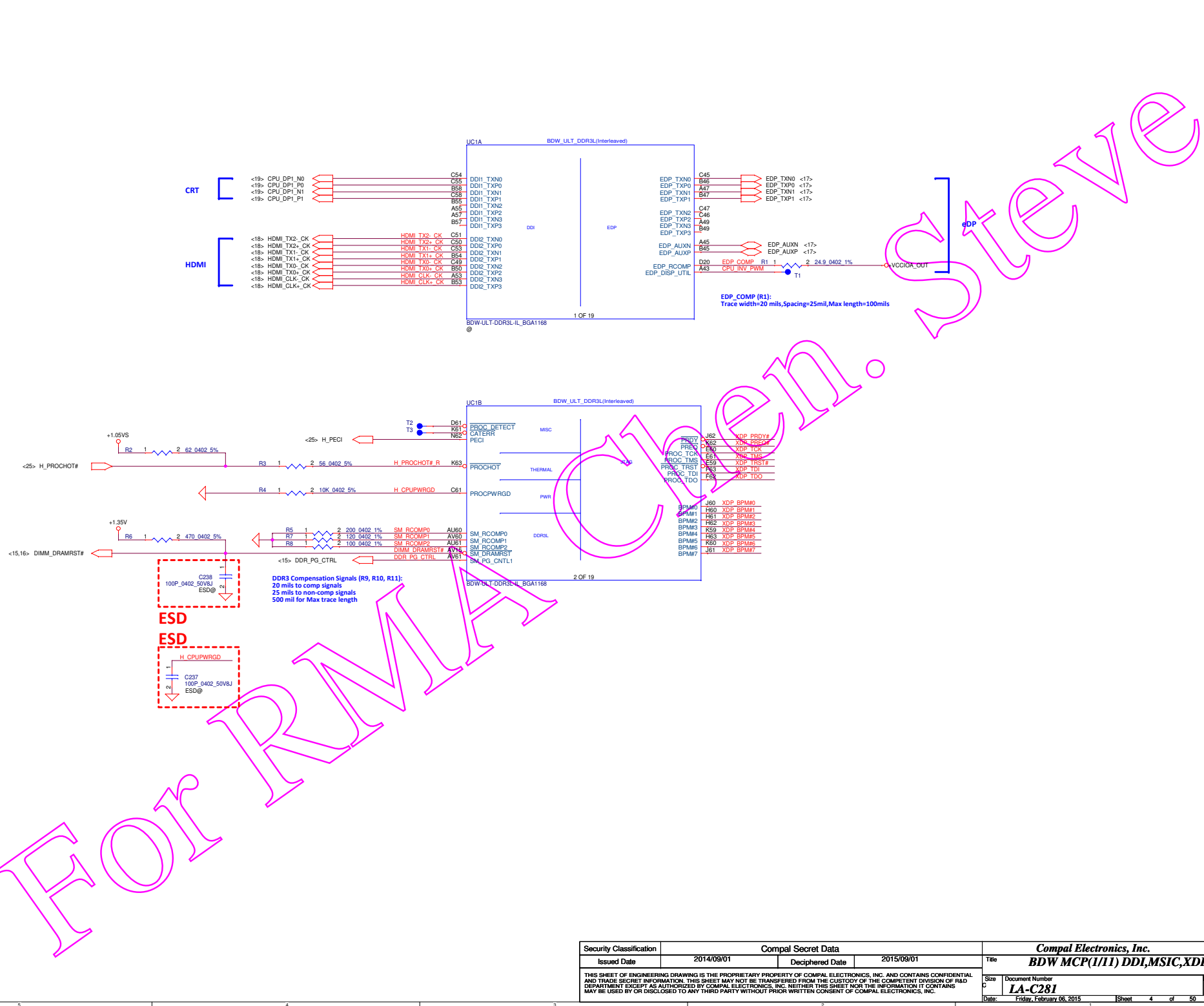
- UC1
SA000089A60 17-5500U
S IC FH8065801620004 SR23W F0 2.4G C38!
17_5500@
- UC1
SA000089970 15-5200U
S IC FH8065801620204 SR23Y F0 2.2G C38!
15_5200@
- UC1
SA000089880 13-5010U
S IC FH8065801620406 SR23Z F0 2.1G C38!
13_5010@
- UC1
SA000083EH0 13-5005U
S IC FH8065801884006 SR244 F0 2G C38!
13_5005@

PCB

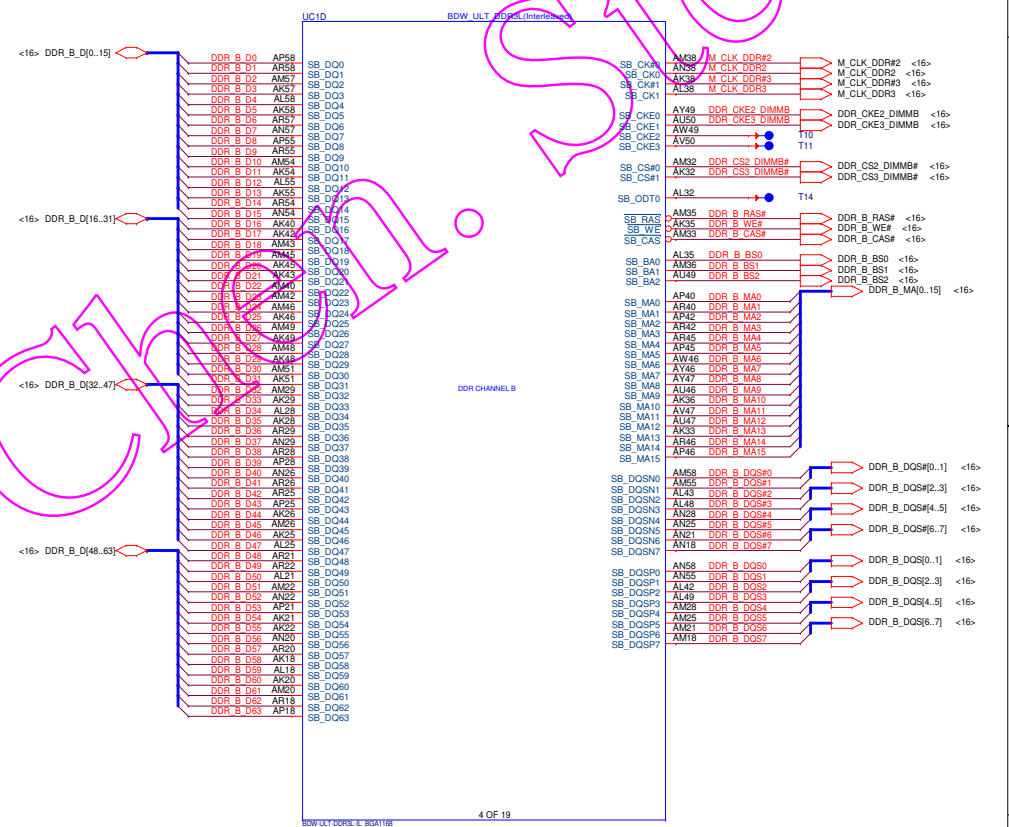
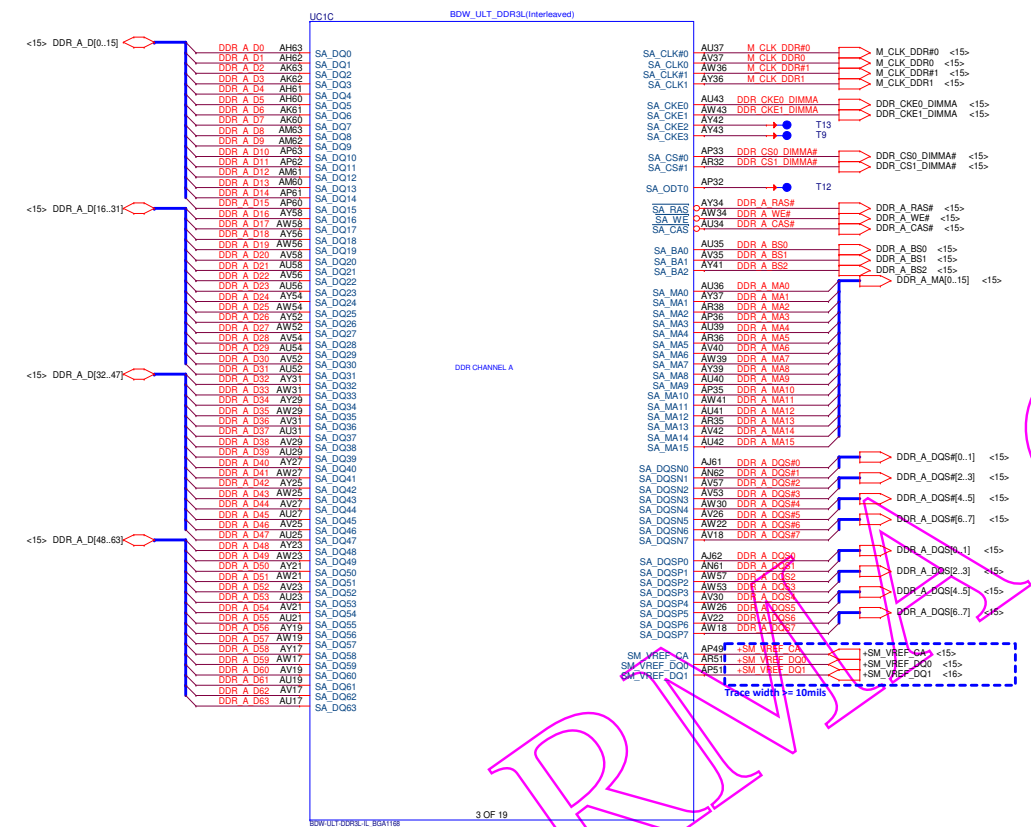
- Z2Z
DA218K00101
PCB AIWZ0 LA-C281P LS-C281P/C282P 02
Z14@
PCB AIWZ0 LA-C281P LS-C281P/C282P 02
- Z2Z
DA218J00101
PCB AIWZ1 LA-C281P LS-C281P/C282P/C283P/C285P/C286P 02
Z15@
PCB AIWZ1 LA-C281P LS-C281P/C282P/C283P/C285P/C286P 02

BOM Structure Table

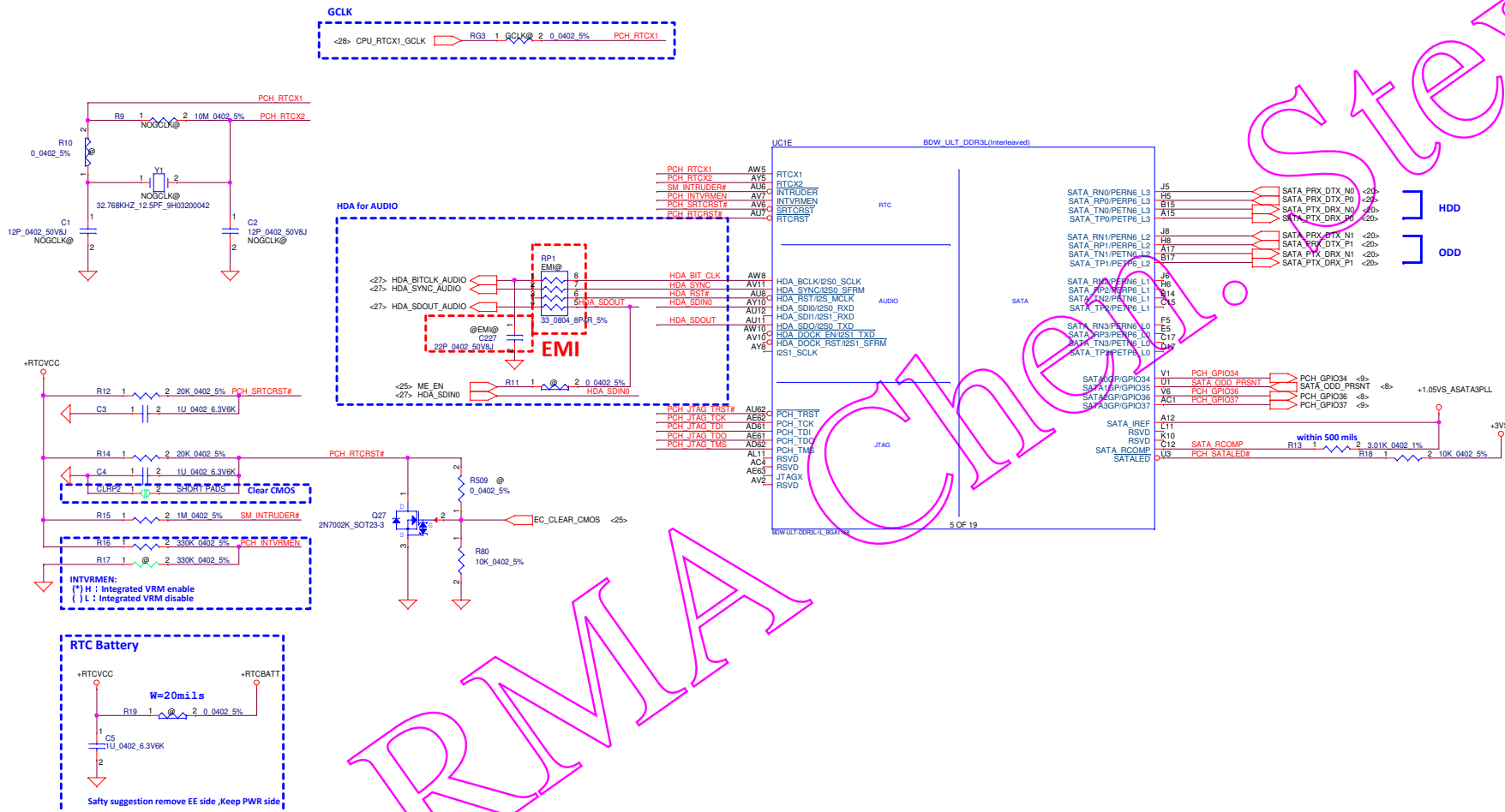
Item	BOM Structure
AIWZ0 (14")	Z14@
AIWZ1 (15")	Z15@
AIWZ0 (17")	Z17@
LAN Switch mode	SWITCH@
LAN RTL811GS-CG	8111GLDO@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NOISCT@
For Green CLK	GCLK@
For No Green CLK	NOGCLK@
Green CLK IC For DIS	GCLKDIS@
Green CLK IC For UMA	GCLKUMA@
For system DIS	PX@
For TROPO DIS pop	DIS@
For TROPO DIS unpop	@DIS@
For UMA	UMA@
3D Camera	3DCMOS@
Camera	CMOS@
HDMI	HDMI@
NO keyboard backlight	NOKBL@
Keyboard backlight	KBL@
HDMI Royalty	45@
Connector	ME@
Un-pop component for EMI	@EMI@
Un-pop component for ESD	@ESD@
pop component for EMI	EMI@
pop component for ESD	ESD@
Un-pop for TPM	TPM@
pop for TPM	NOTPM@
VRAM identify	X76@
For TROPO function	TROPO@
ADB function	ADB@
NO ADB function	NOADB@
CPU_SA000083E30	QGZ3@
CPU_SA000083C10	QH17@
CPU_SA00007AM00	QFSY@
CPU_SA000083A10	QH15@
CPU_SA000083D30	QH18@
CPU_SA00007UG00	QGHA@
CPU_SA00007UH00	QGH@
CPU_SA00007U900	QGH9@

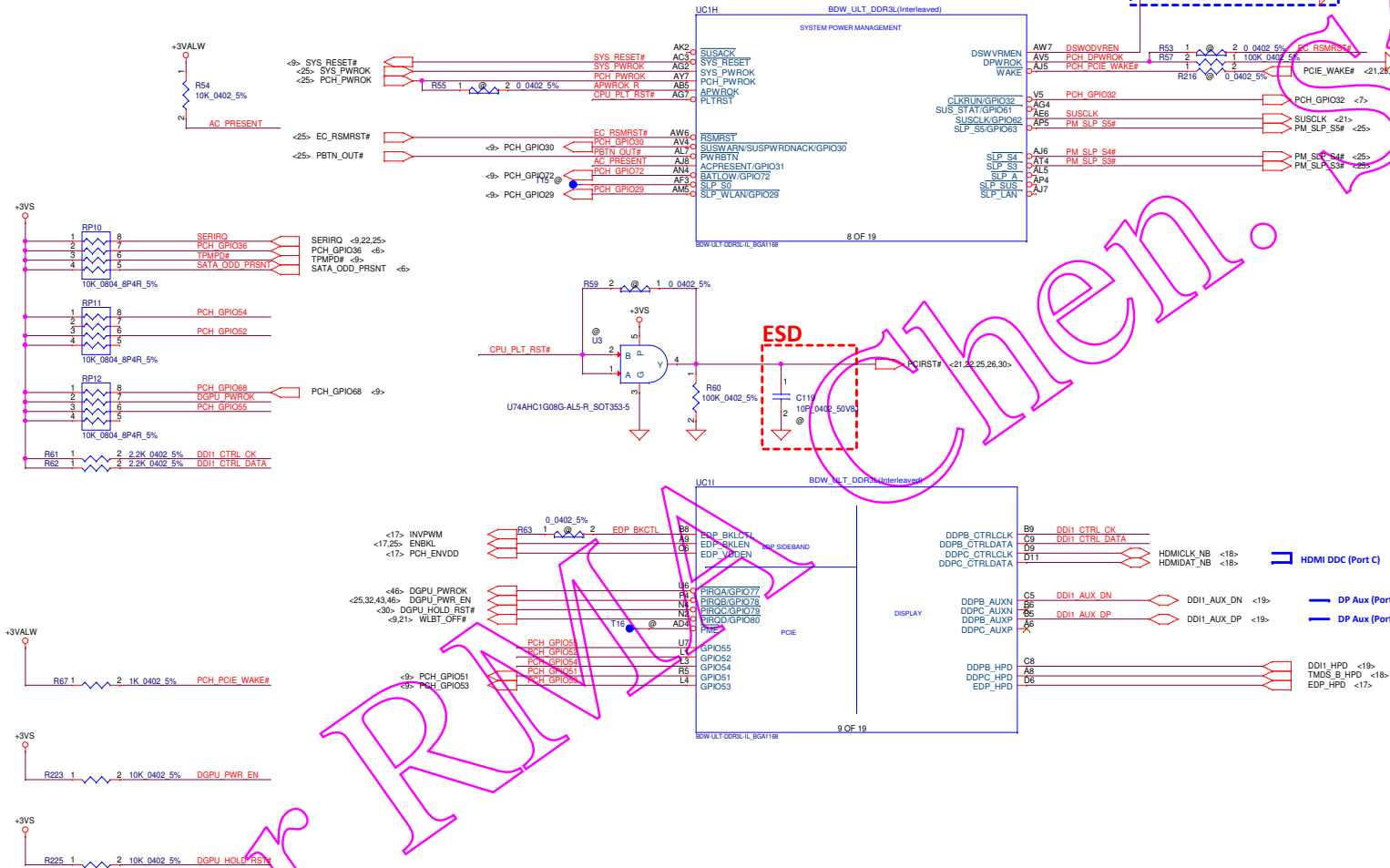
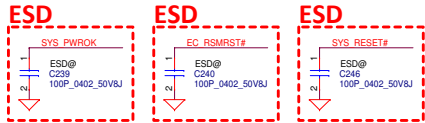


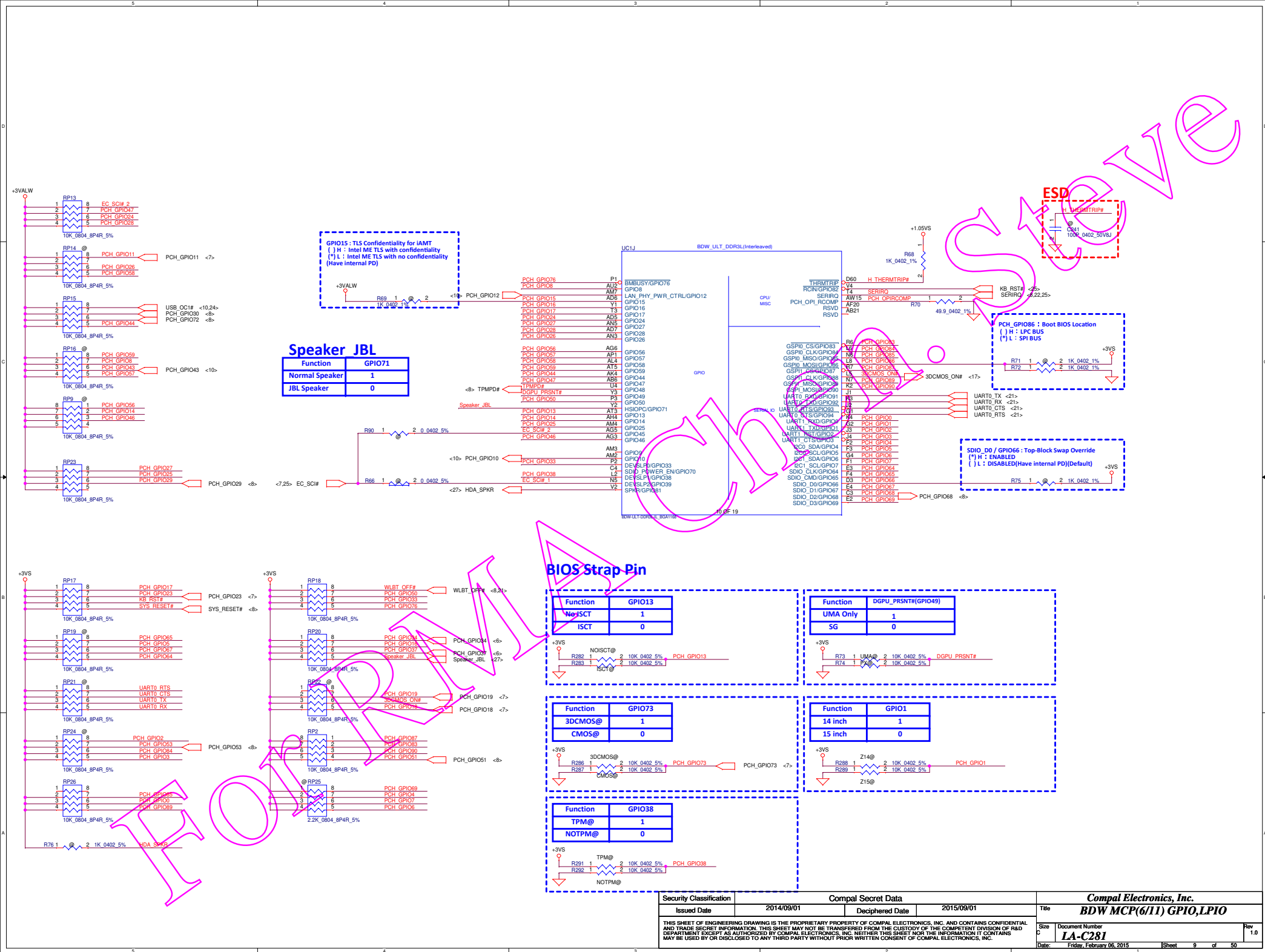
Interleaved Memory



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GPIO15 : TLS Confidentiality for IAMT
(*) H : Intel ME TLS with confidentiality
(*) L : Intel ME TLS with no confidentiality
(Have Internal PD)

Speaker JBL	
Function	GPIO71
Normal Speaker	1
JBL Speaker	0

BIOS Strap Pin

Function	GPIO13
WdgISCT	1
ISCT	0

Function	GPIO73
3DCMOS@	1
CMOS@	0

Function	GPIO38
TPM@	1
NOTPM@	0

Function	DGPU_PRSTN(GPIO49)
UMA Only	1
SG	0

Function	GPIO1
14 inch	1
15 inch	0

dGPU

LAN

WLAN

3D Camera

<30> PCIE_CRX_GTX_N0
<30> PCIE_CRX_GTX_P0
<30> PCIE_CTX_GRX_N0
<30> PCIE_CTX_GRX_P0
<30> PCIE_CRX_GTX_N1
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<30> PCIE_CRX_GTX_P2
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<30> PCIE_CTX_GRX_P2
<30> PCIE_CRX_GTX_N3
<30> PCIE_CRX_GTX_P3
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<26> PCIE_PRX_DTX_N3
<26> PCIE_PRX_DTX_P3

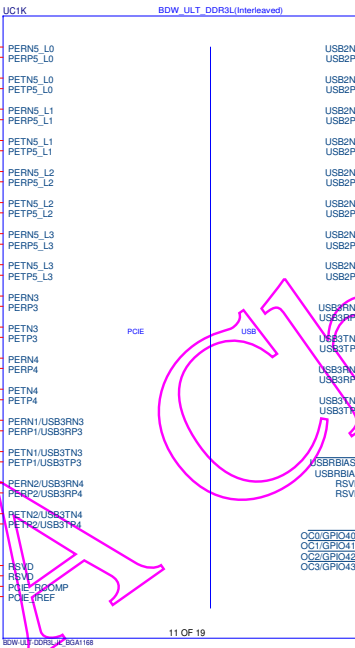
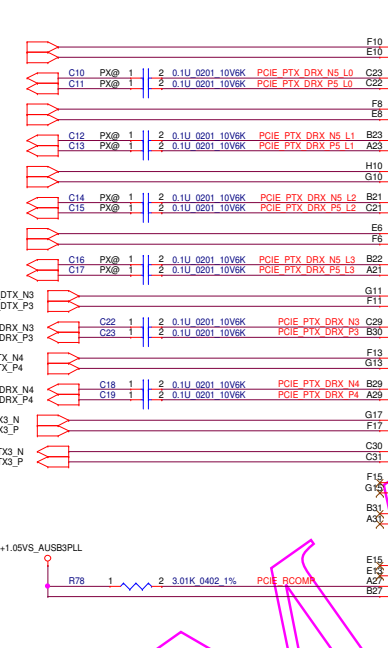
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<26> PCIE_PTX_C_DRX_P3

<21> PCIE_PRX_DTX_N4
<21> PCIE_PRX_DTX_P4

<21> PCIE_PTX_C_DRX_N4
<21> PCIE_PTX_C_DRX_P4

<17> USB3_RX3_N
<17> USB3_RX3_P

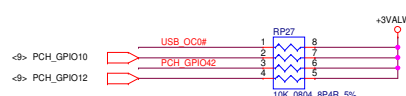
<17> USB3_TX3_N
<17> USB3_TX3_P



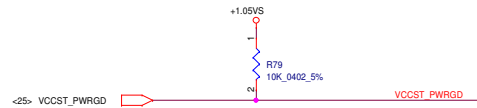
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USB20_P0 <24>
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USB20_P1 <24>
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USB20_P2 <24>
USB20_N3 <24>
USB20_P3 <24>
USB20_N4 <17>
USB20_P4 <17>
USB20_N5 <17>
USB20_P5 <17>
USB20_N6 <21>
USB20_P6 <21>
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USB3_RX1_P <24>
USB3_TX1_N <24>
USB3_TX1_P <24>
USB3_RX2_N <24>
USB3_RX2_P <24>
USB3_TX2_N <24>
USB3_TX2_P <24>
USB_OC0# <24>
USB_OC1# <24>
PCH_GPIO42 <9>
PCH_GPIO43 <9>

Left USB2/3_I/O Port (Near End User)
Left USB2/3_I/O Port (Near HDMI CONN)(Debug Port)
Right USB2_I/O Port (Sub Board)
Right USB2 CardReader
Touch Screen
Camera
Bluetooth (NGFF)
Left USB2/3_I/O Port
Left USB2/3_I/O Port
Left USB2/3_I/O Port

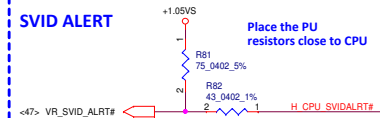
CAD note:
Route single-end 50-ohms and max 450-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils



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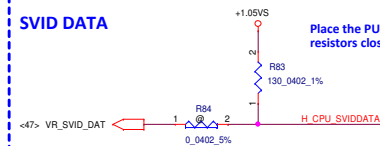


SVID ALERT

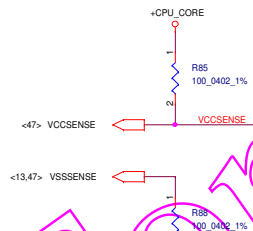


Place the PU resistors close to CPU

SVID DATA



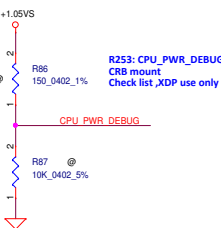
Place the PU resistors close to CPU



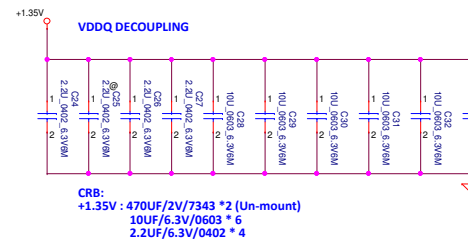
PU resistor should be close to CPU



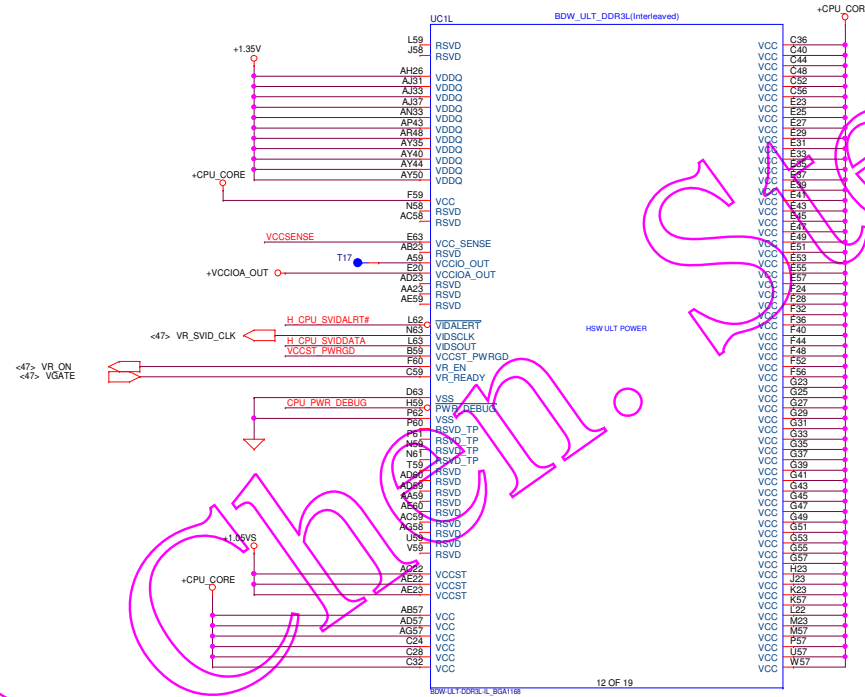
PD resistor should be close to CPU



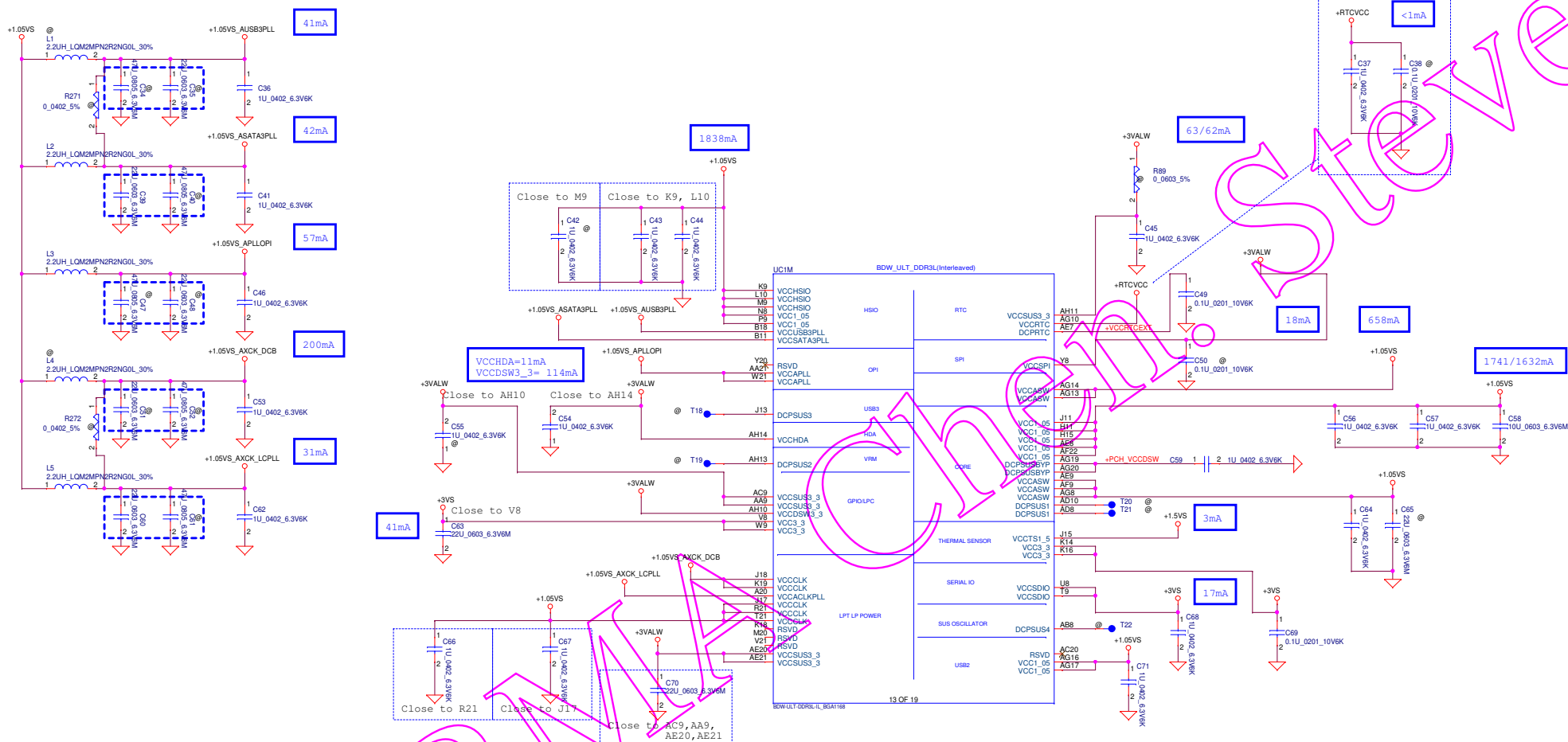
R253: CPU_PWR_DEBUG
CRB mount
Check list_XDP use only



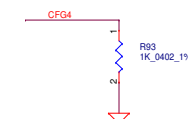
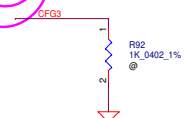
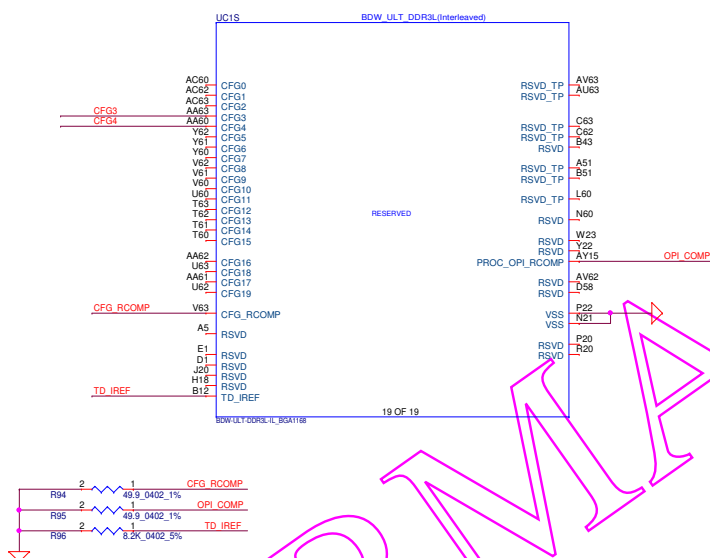
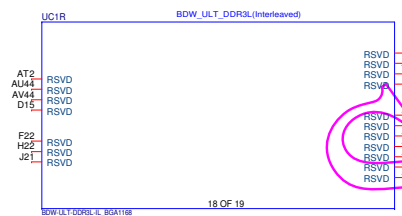
CRB:
+1.35V : 470UF/2V/7343 *2 (Un-mount)
10UF/6.3V/0603 *6
2.2UF/6.3V/0402 *4



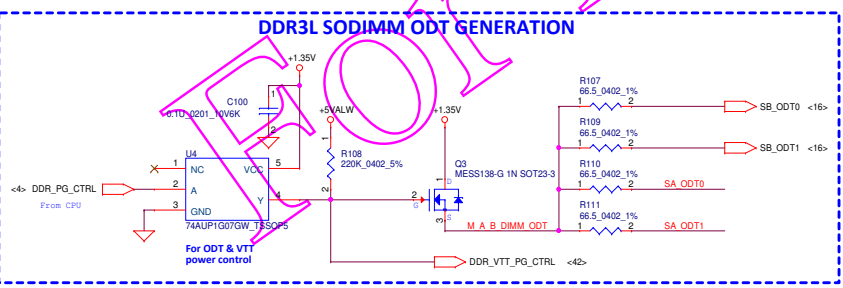
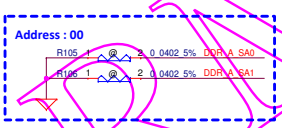
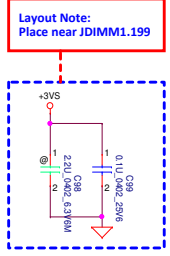
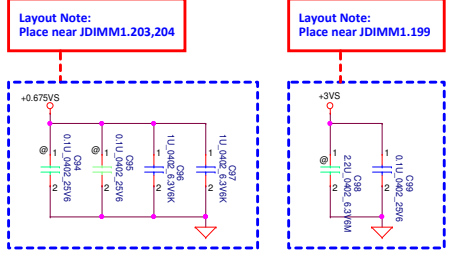
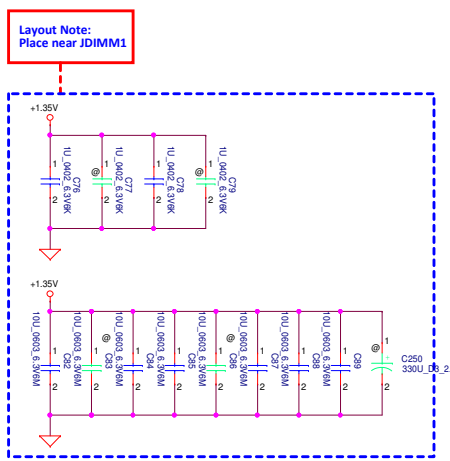
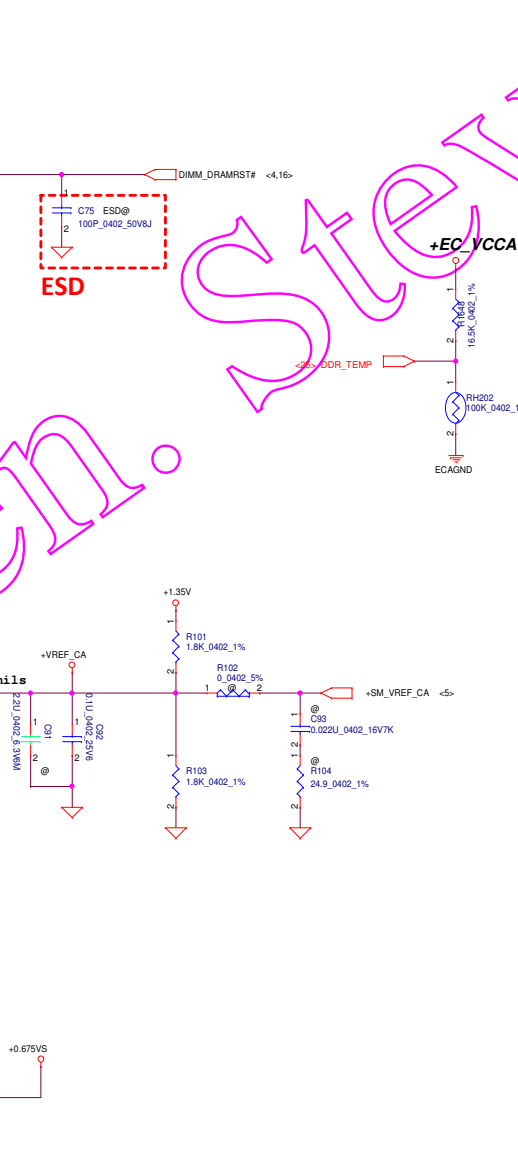
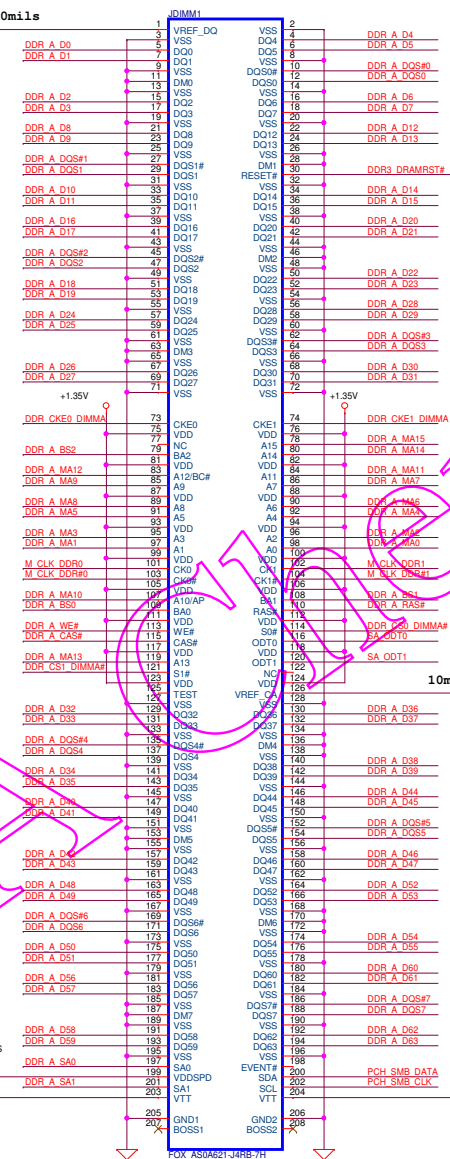
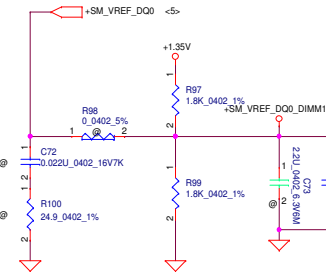
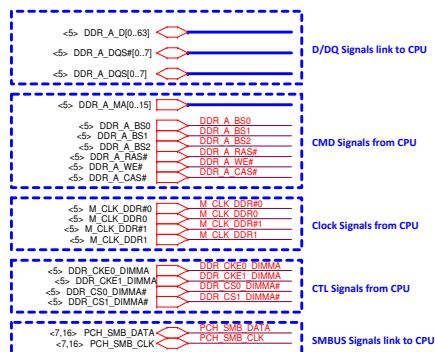
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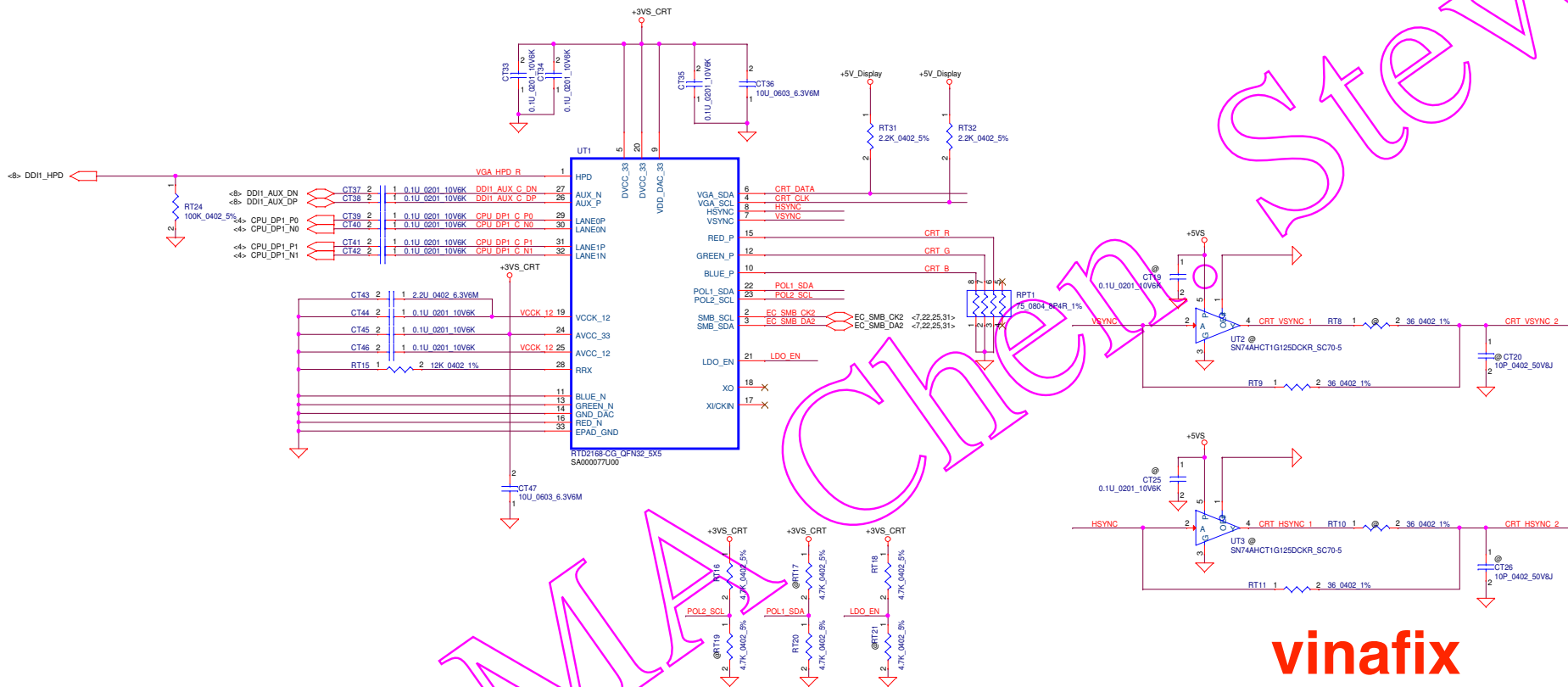
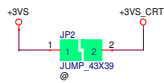
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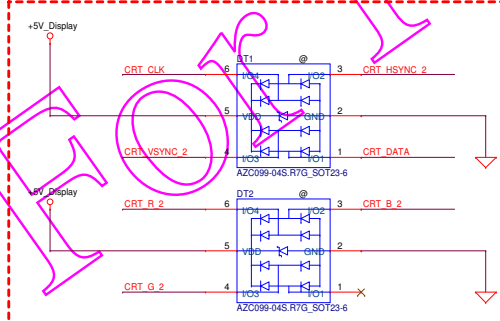
DIMM1
Dimmer Type
Near CPU



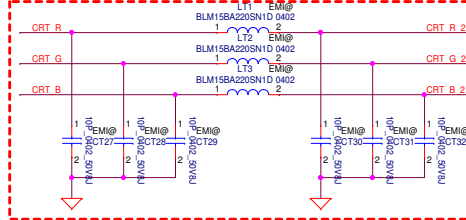
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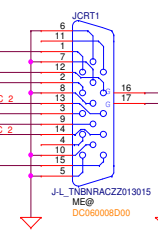
ESD



EMI

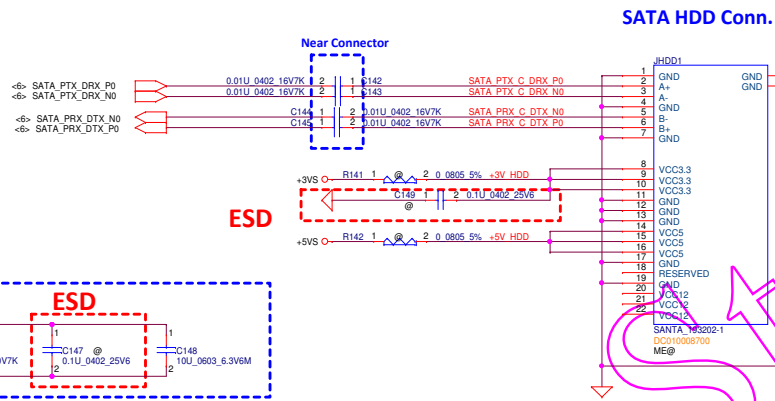


CRT

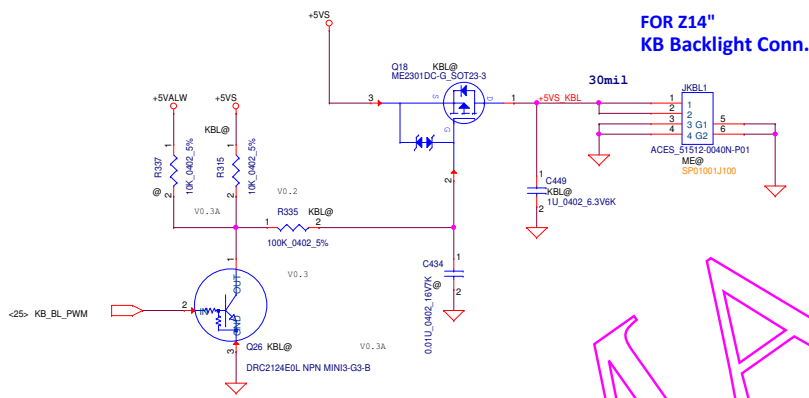


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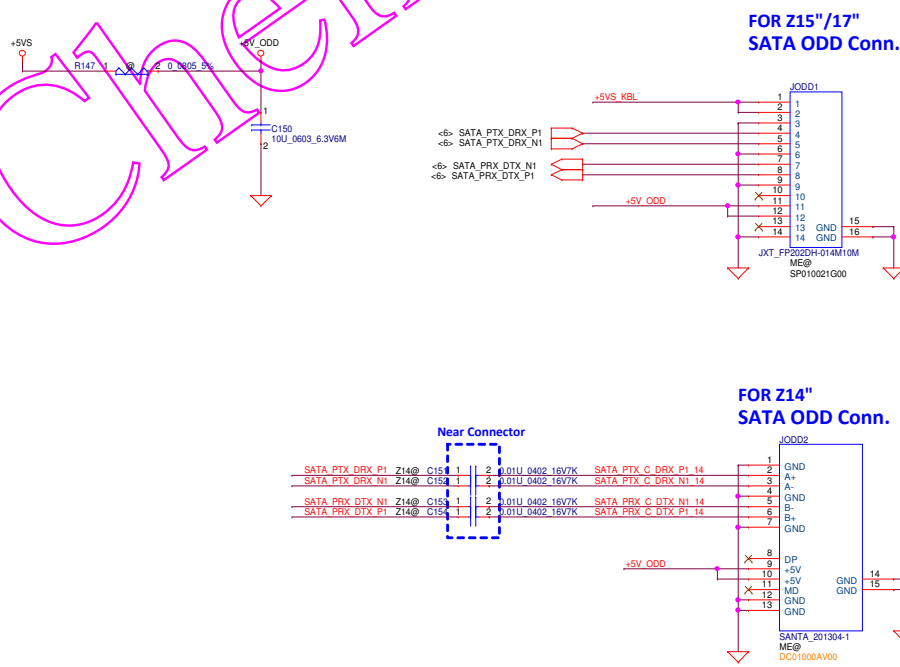
HDD



KB Backlight



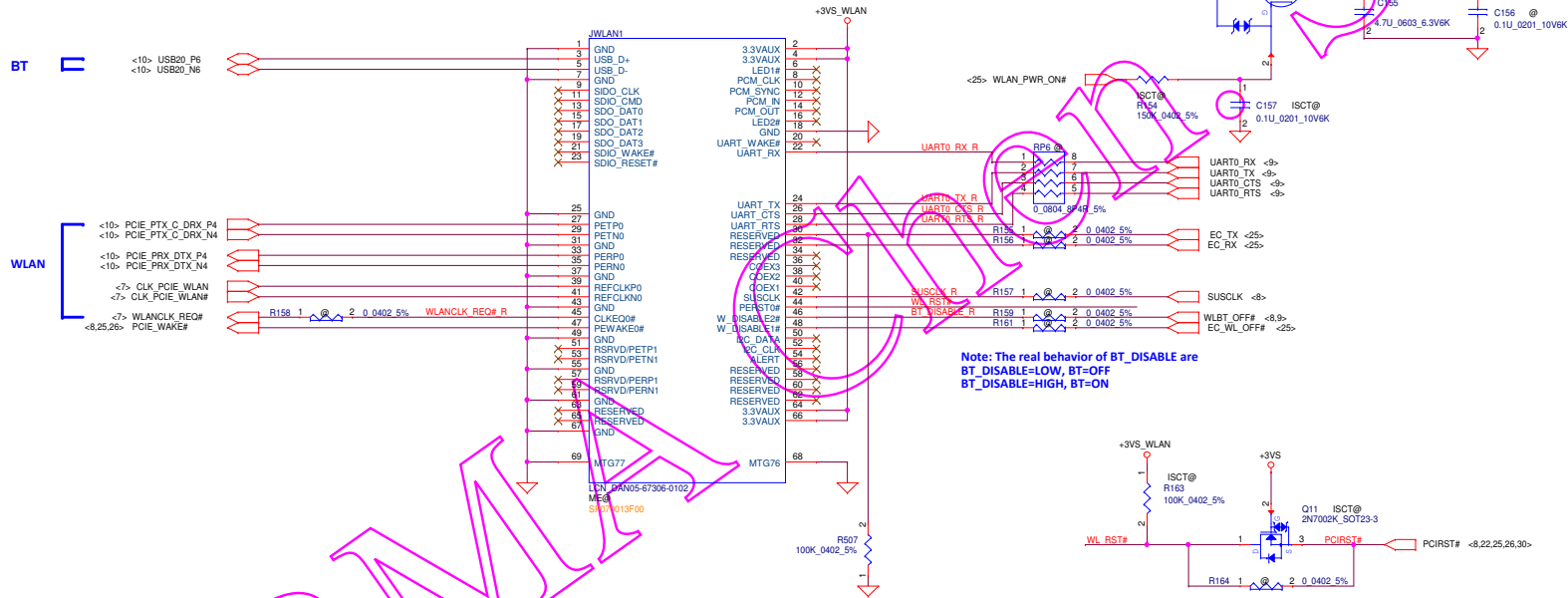
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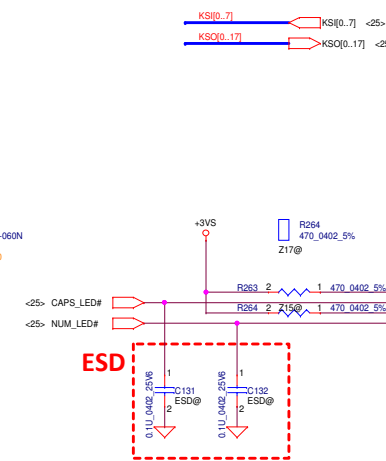
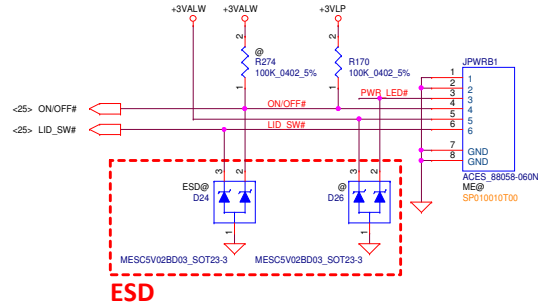
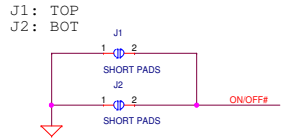
For RMA

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NGFF for WLAN / BT(Key E) Support ISCT(Intel Smart Connect Technology)



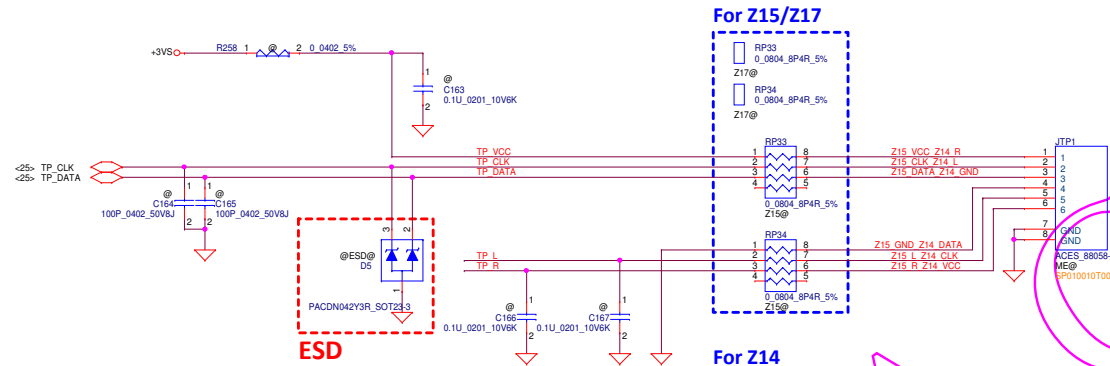
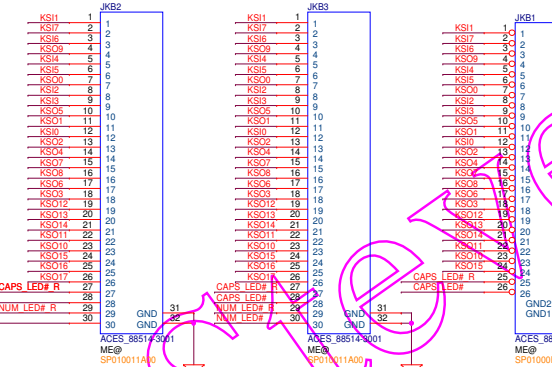
vinafix



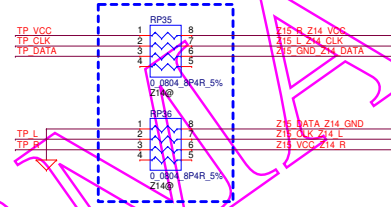
KB For Z15

KB For Z17

KB For Z14



For Z14



For Z14,Z15,Z17 TP module(100*50)

1	1	VCC
2	2	CLK
3	3	DAT
4	4	GND
5	5	L
6	6	R

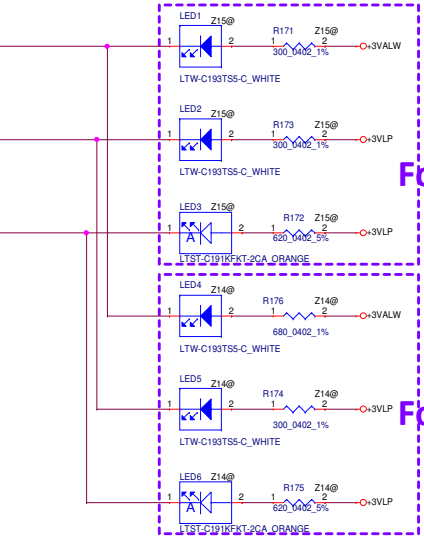
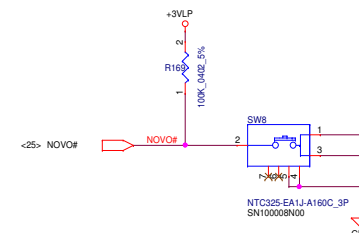
MB TP module

For Z14 TP module(100*50)

6	1	VCC
5	2	CLK
4	3	DAT
3	4	GND
2	5	L
1	6	R

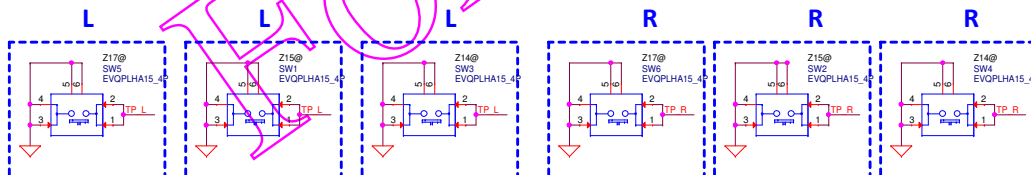
MB TP module

NOVO

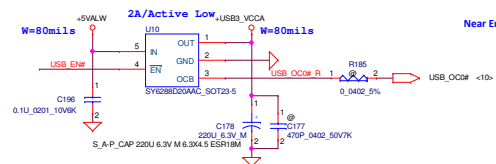
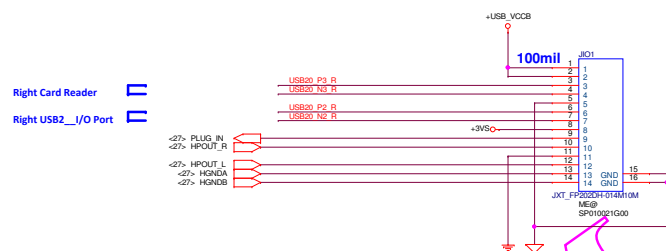


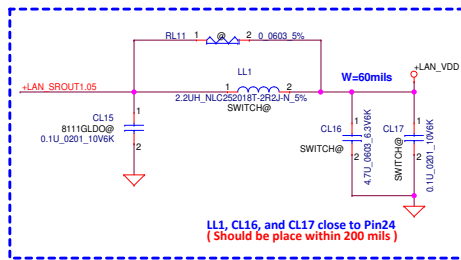
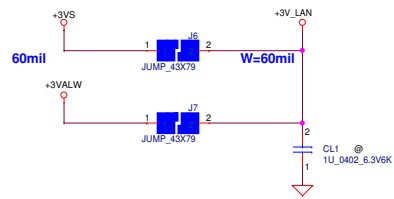
For Z15

For Z14



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ROM/KB/D/PWR/CR/LED/TP Conn.		
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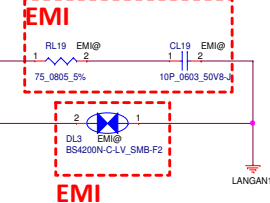
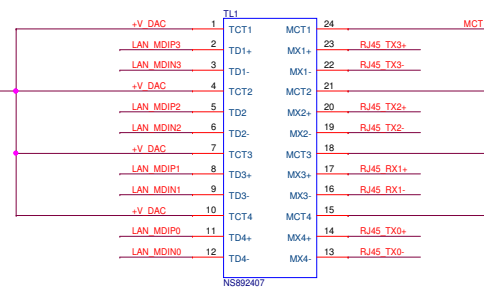
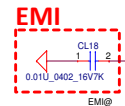
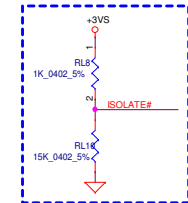
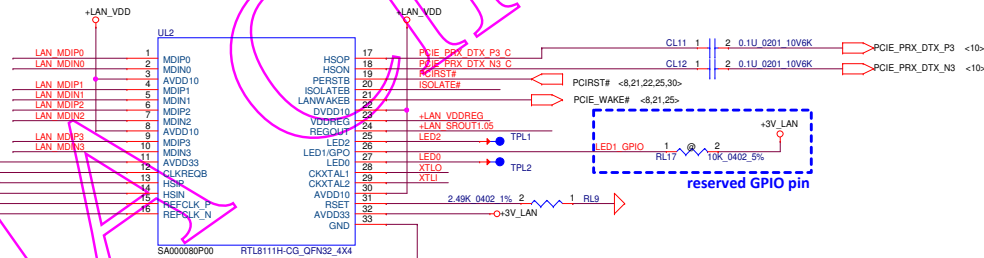
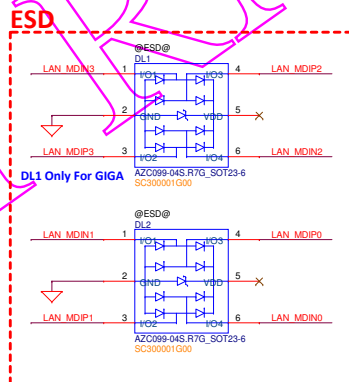
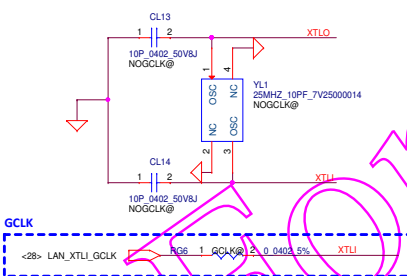
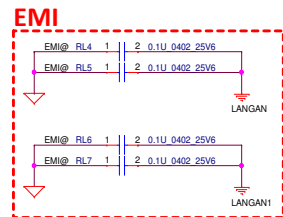
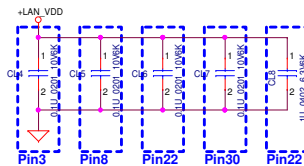
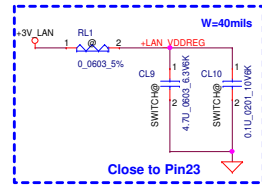
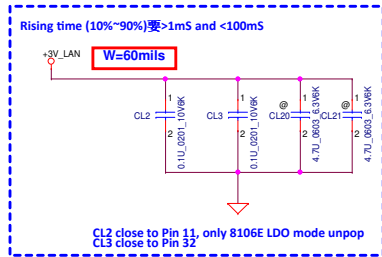
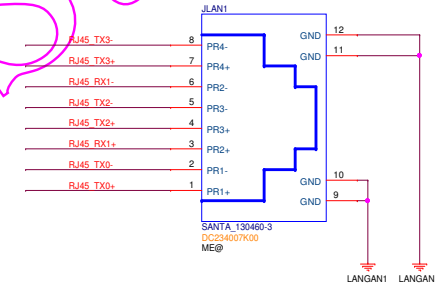
SA00005V700

SA000005Y00

	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111G	LDO	X	X	X	O	O
RTL8111G	External	X	X	X	X	O
RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
RTL8106E	LDO	X	X	X	X	X

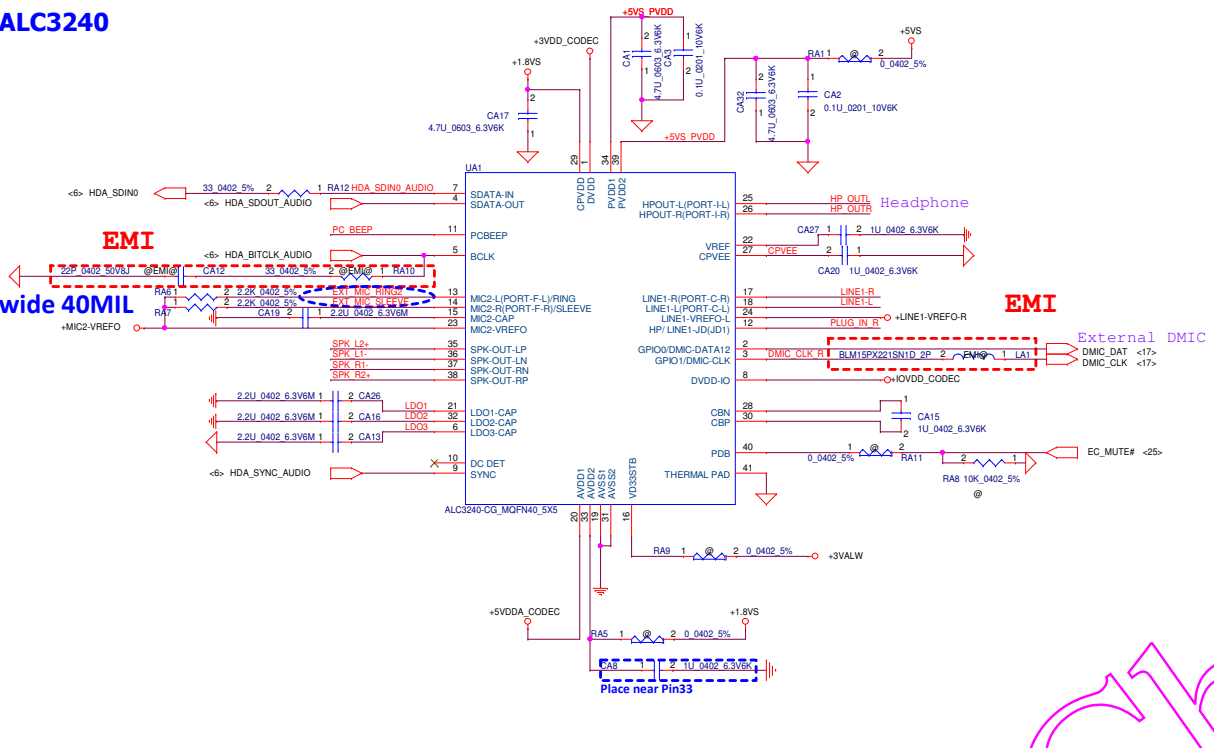
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

RJ-45 CONN.

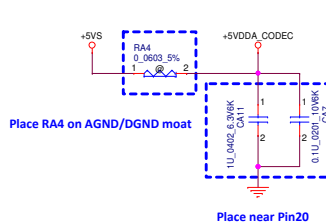


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ALC3240



+5VS → +5VDDA_CODEC



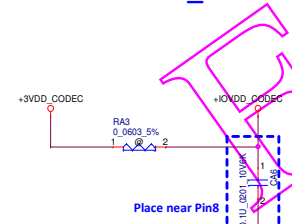
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V	V	V	V	V
Intel Braswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M	V	V	V	V	V

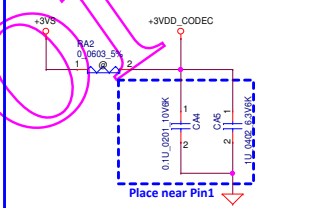
Each Platform HDA Link Voltage Support (Pin 8) :

	3.3V	1.5V
AMD Carrizo		V
AMD Carrizo-L		V
Intel Broadwell	V	V
Intel Braswell	V	V
Intel Skylake	V	V
Intel Bay trail-M		V

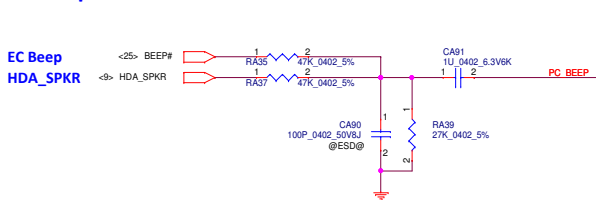
+3VDD_CODEC → +IOVDD_CODEC



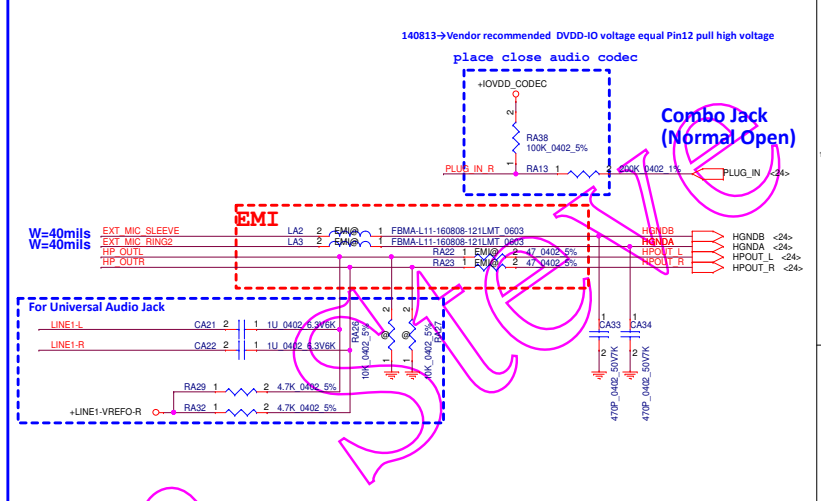
+3VS → +3VDD_CODEC



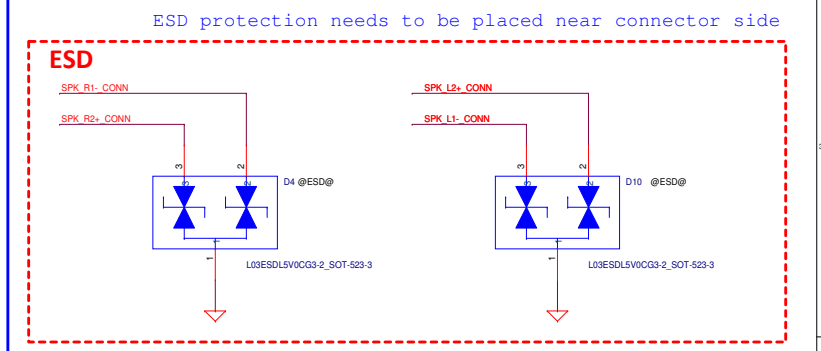
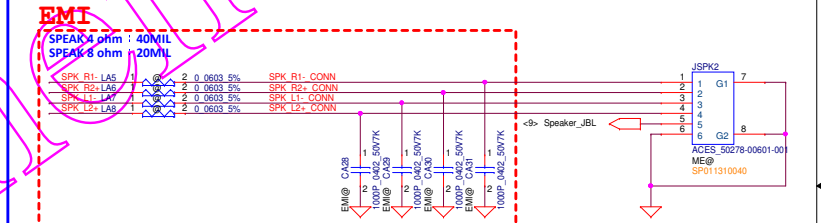
PC Beep



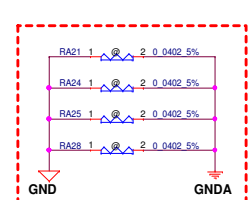
Input



Output

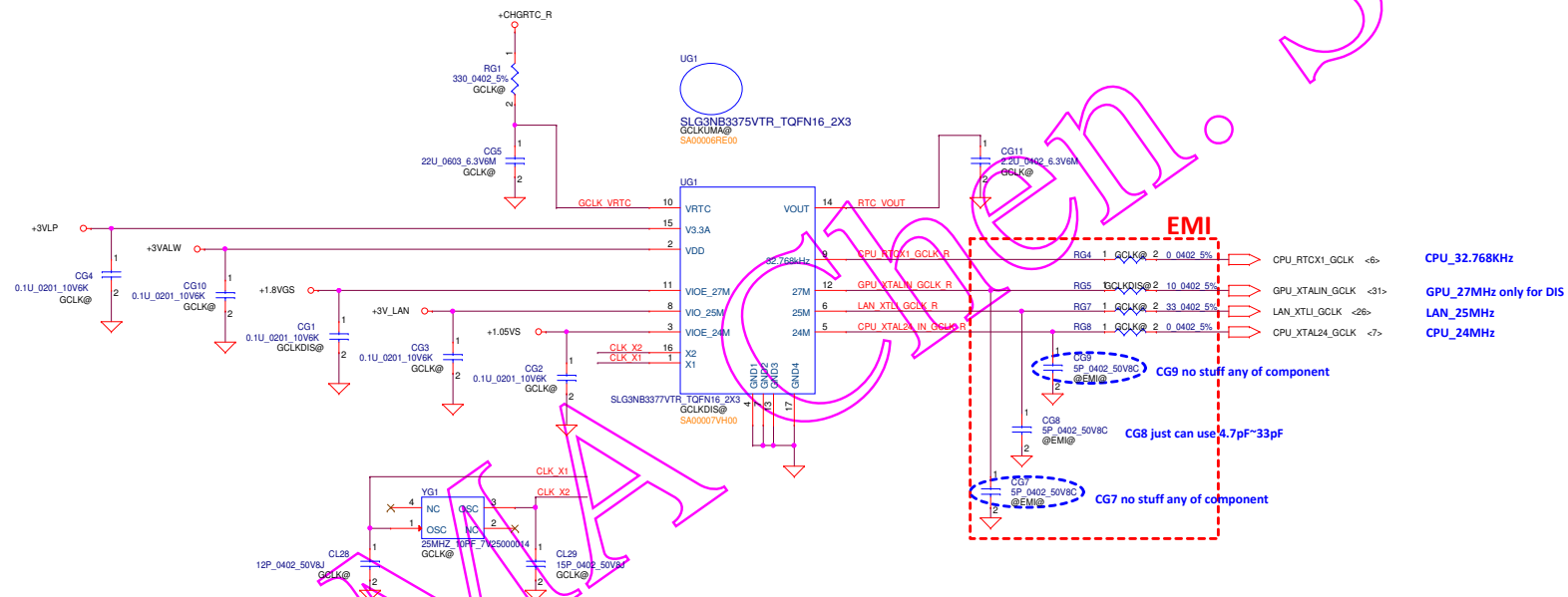


EMI

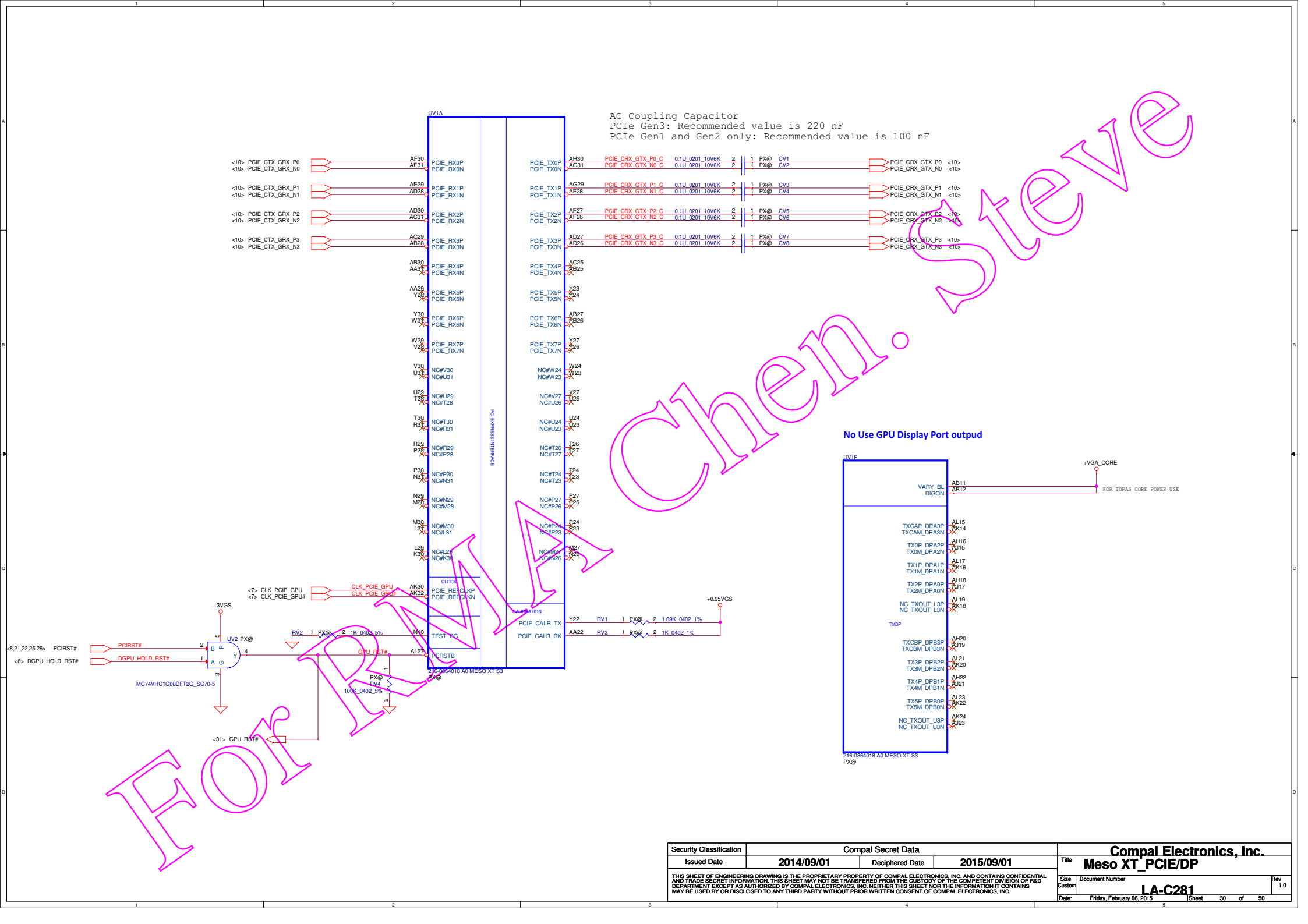


For Review

Compal Steve



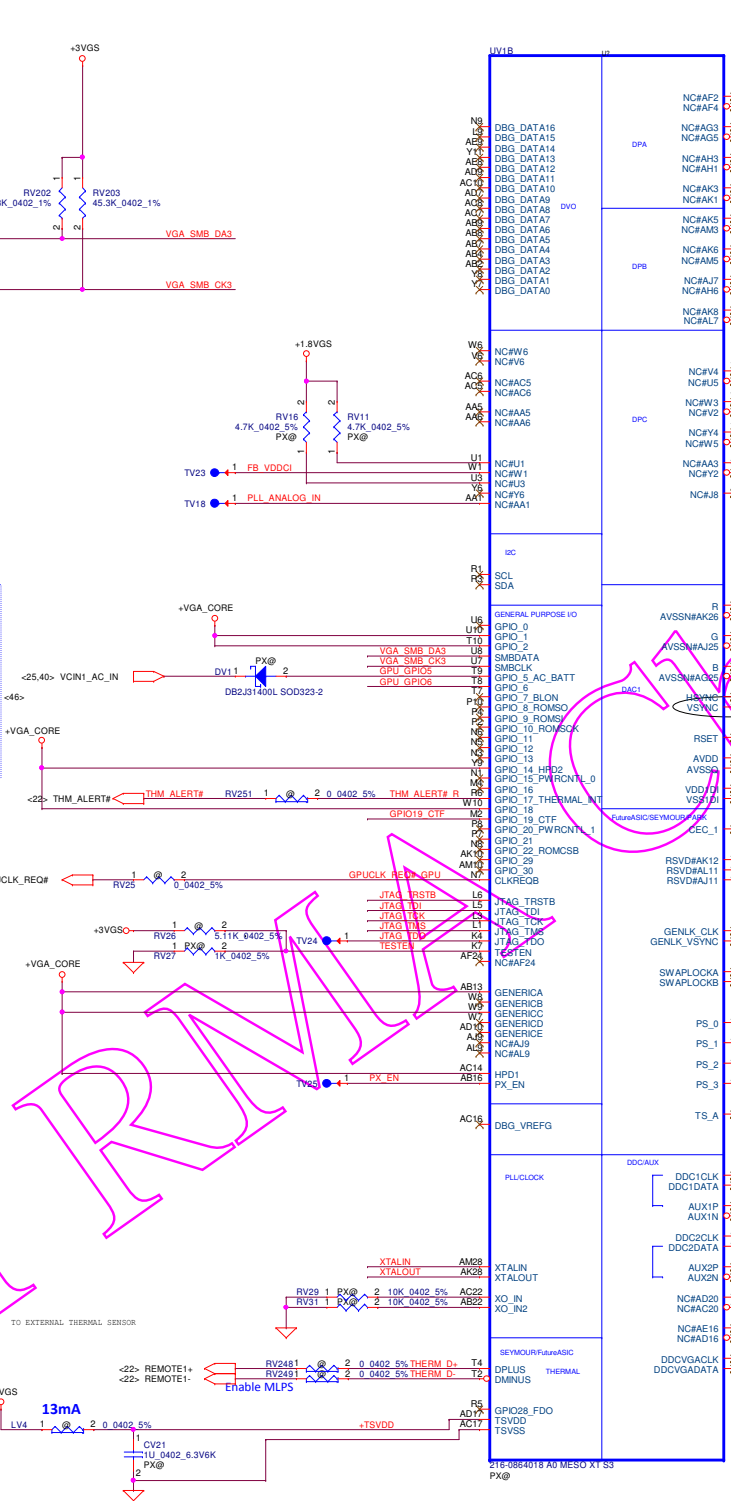
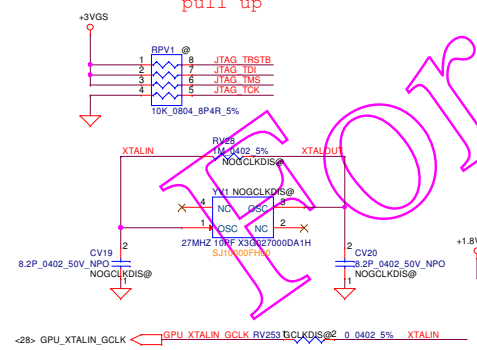
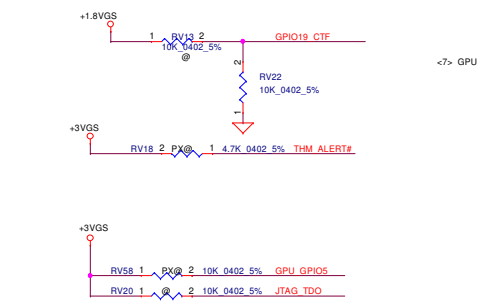
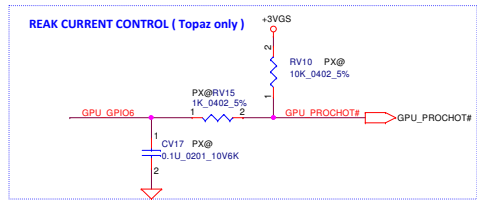
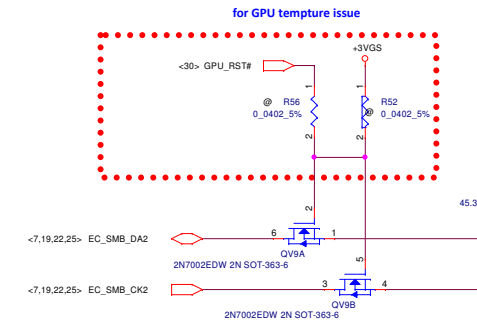
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AC Coupling Capacitor
PCIe Gen3: Recommended value is 220 nF
PCIe Gen1 and Gen2 only: Recommended value is 100 nF

No Use GPU Display Port output

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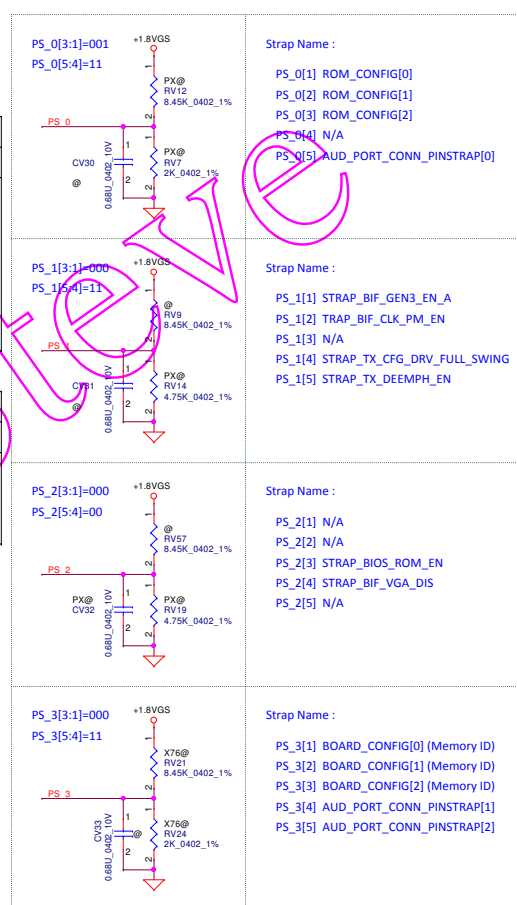
Resistor Divider Lookup Table

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

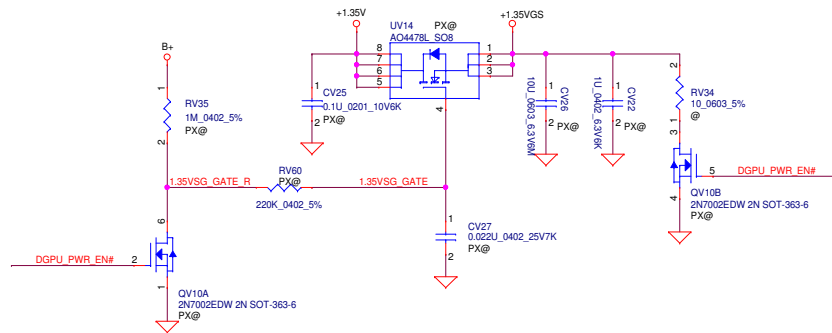
0402 1% resistors are required

Capacitor Divider Lookup Table

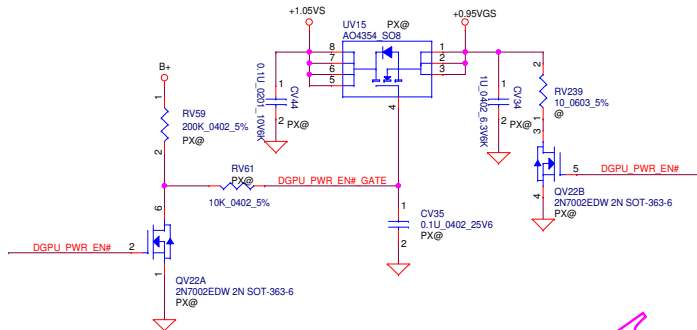
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



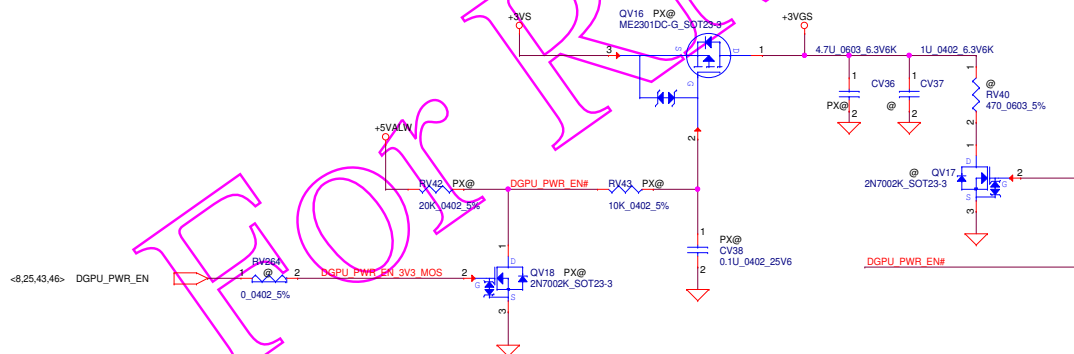
+1.35VS to +1.35VGS (6.234A)



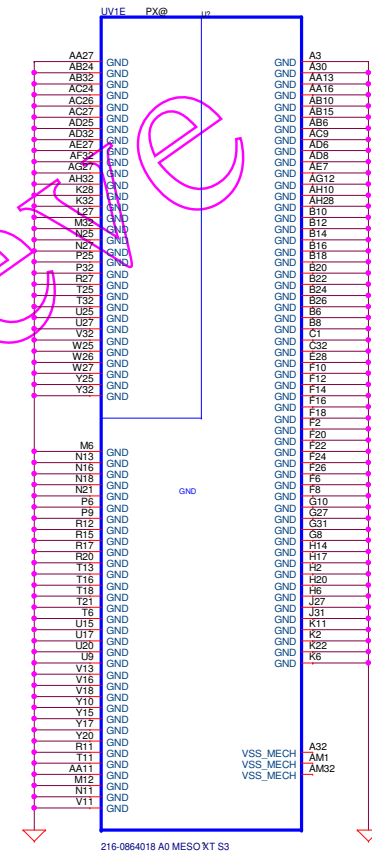
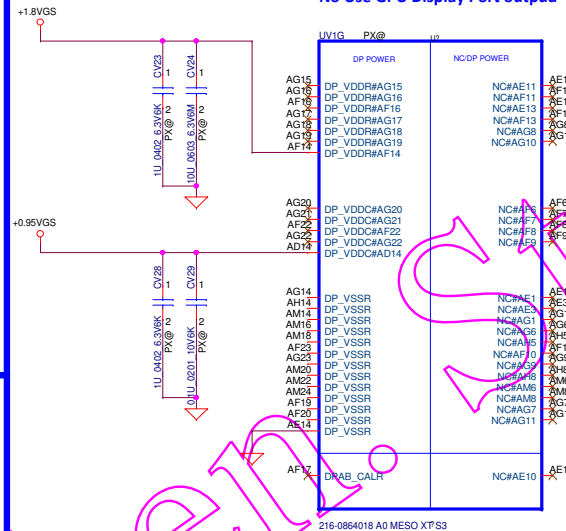
+1.05VS to +0.95VGS



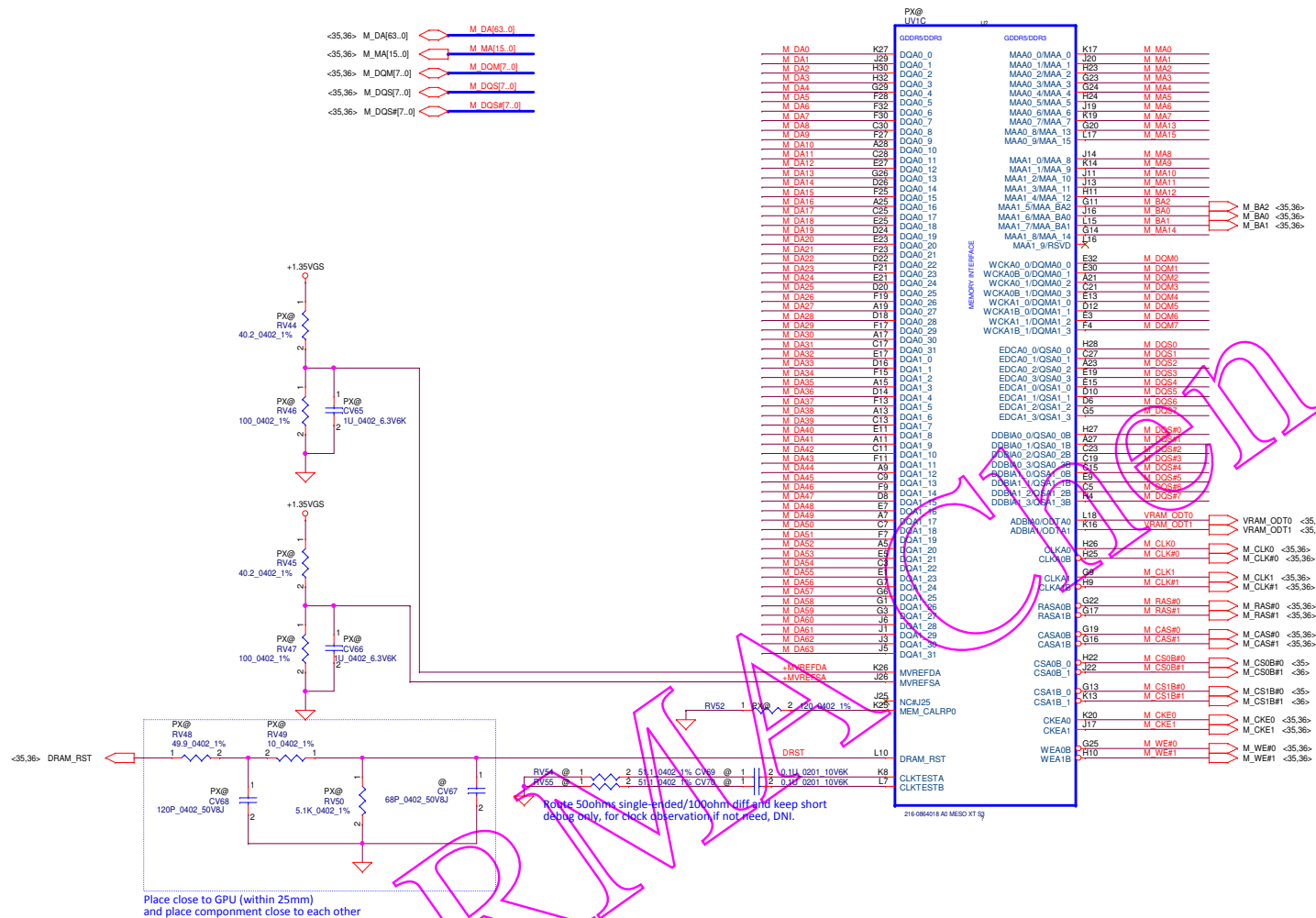
+3VS to +3VS_VGA (25mA)

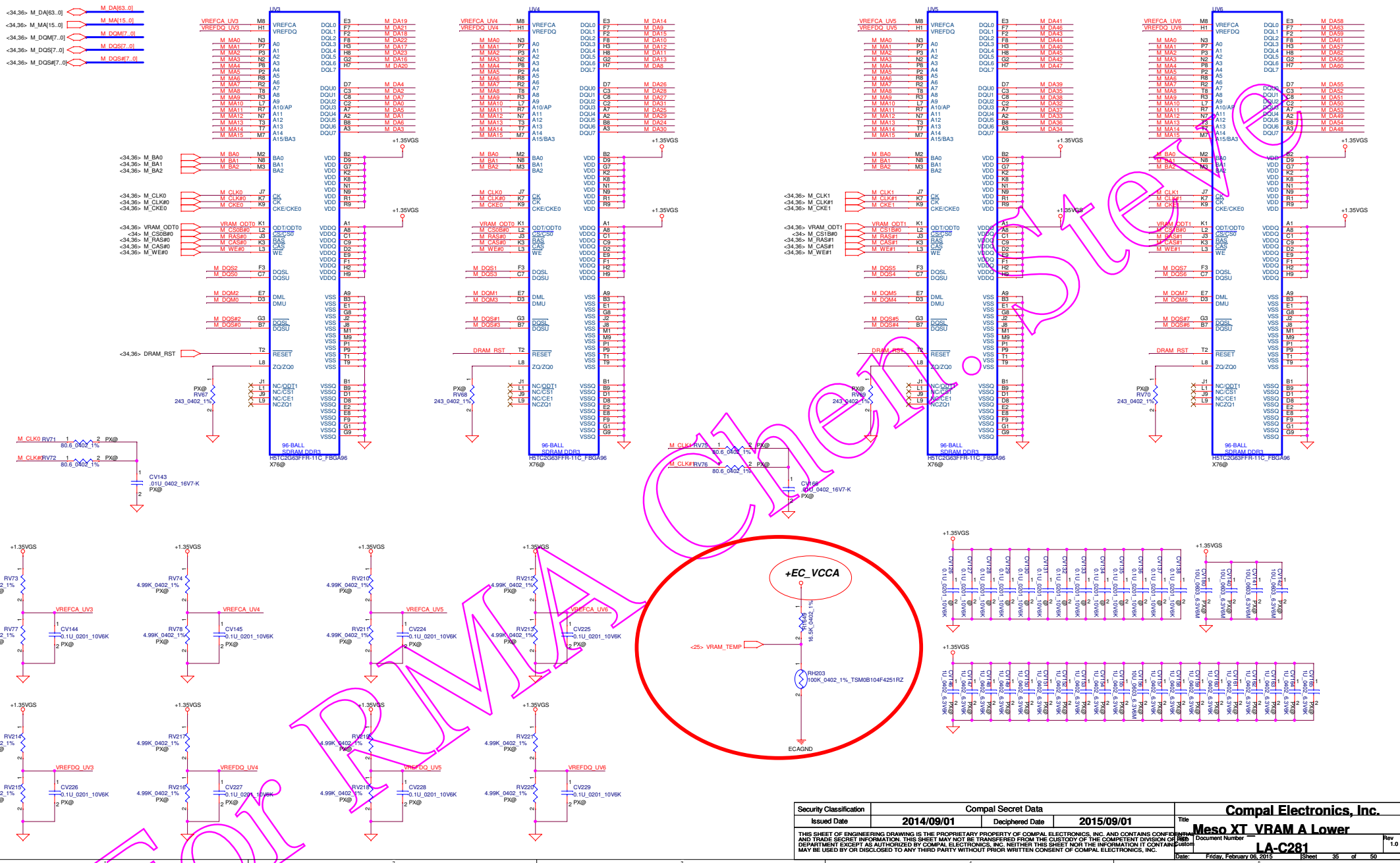


No Use GPU Display Port output



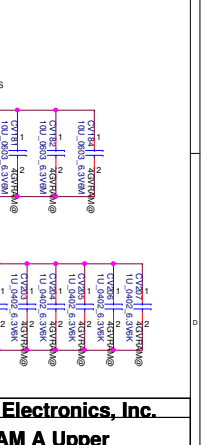
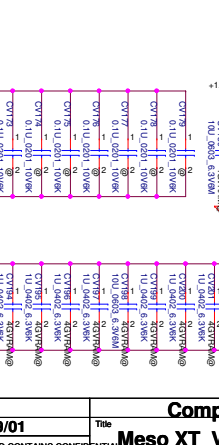
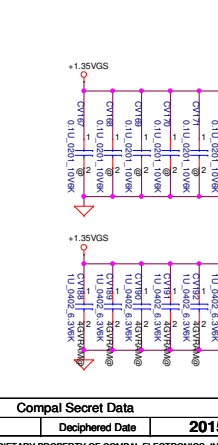
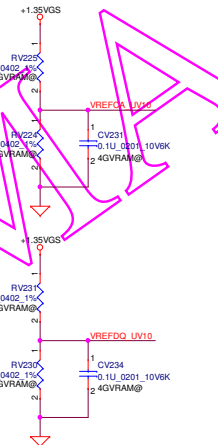
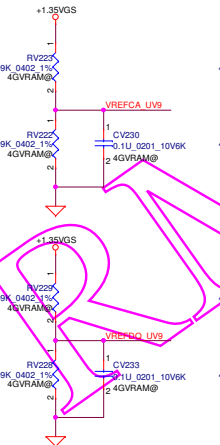
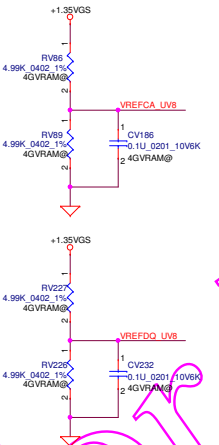
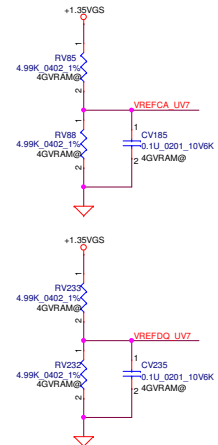
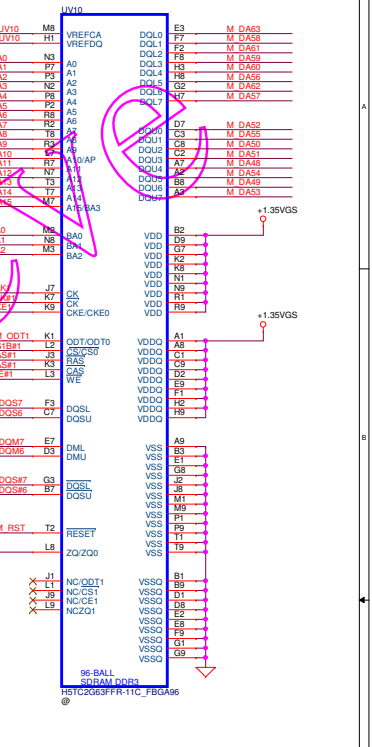
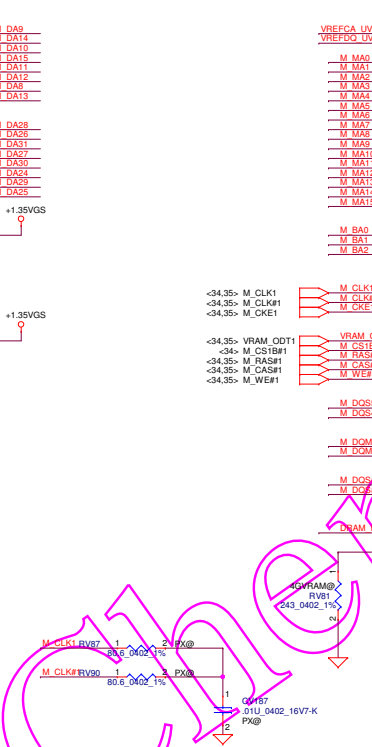
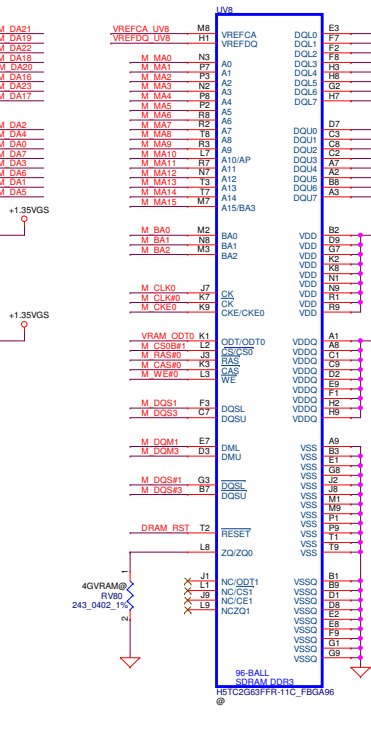
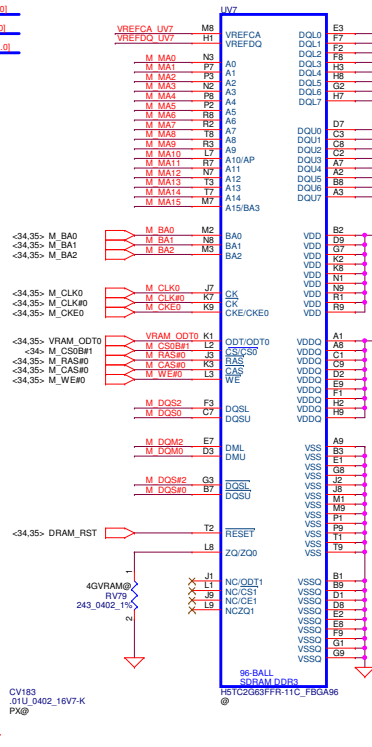
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				Sheet 35 of 50	

<34.35> M_DA[63..0] M_DA[63..0]
<34.35> M_MA[15..0] M_MA[15..0]
<34.35> M_DM[7..0] M_DM[7..0]
<34.35> M_DS[7..0] M_DS[7..0]
<34.35> M_DS[7..0] M_DS[7..0]



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Issued Date	2014/09/01	Deciphered Date	2015/09/01	Meso XT VRAM A Upper
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Meso XT_VRAM_TRAP

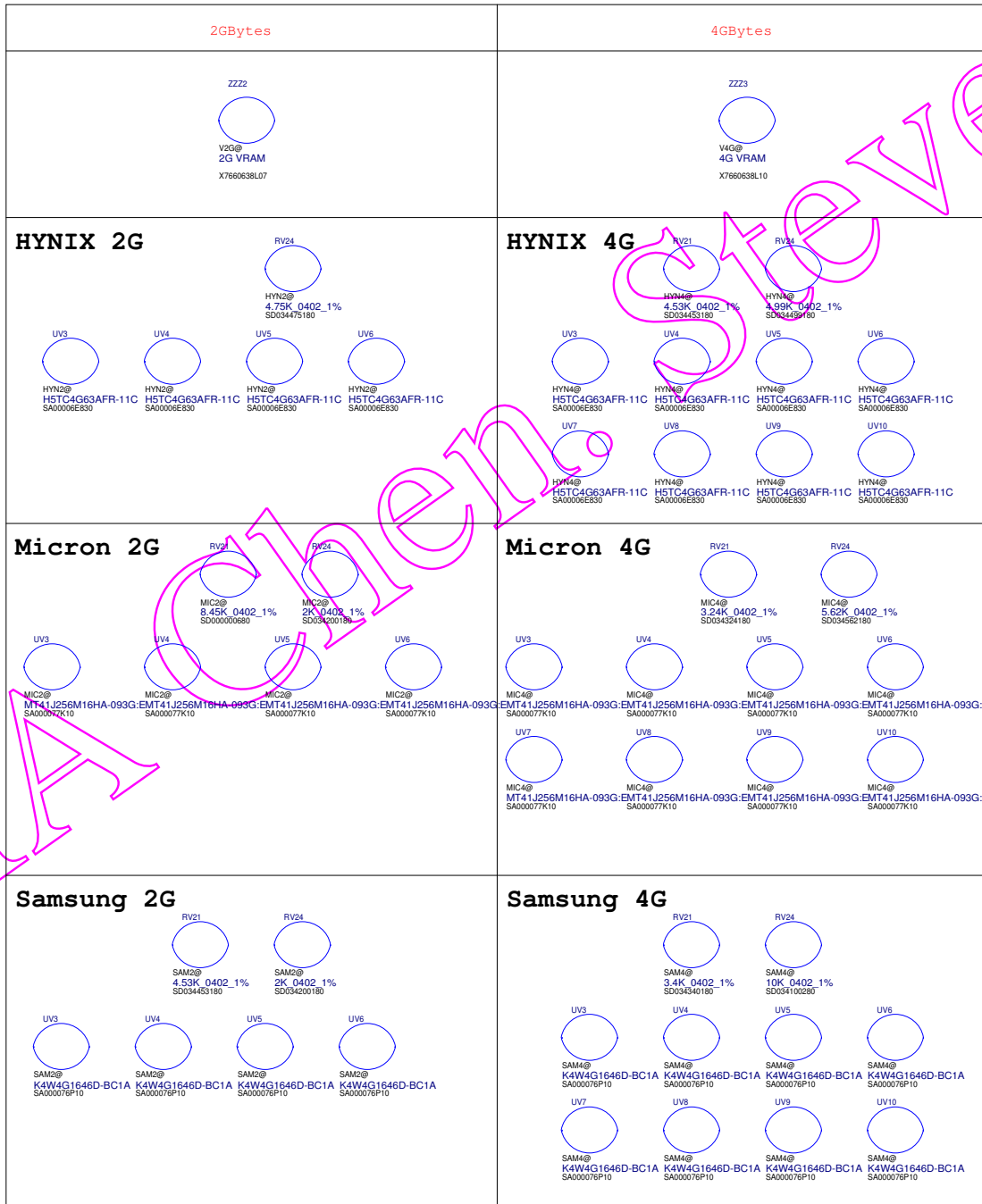
X76@

X76@

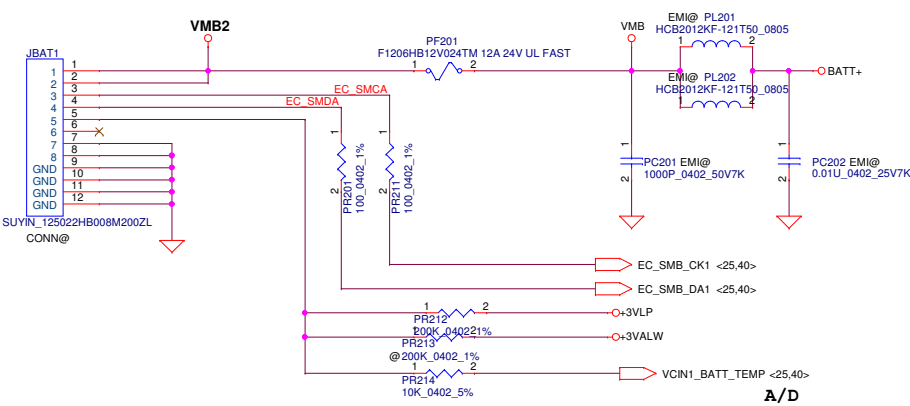
	Vendor	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
						RV21	RV24
2GBytes	UV3, UV4, UV5, UV6, UV7, UV8, UV9, UV10						
HYN2@	Hynix 2G SA00006E830 256Mx16 H5TC4G63AFR-11C	0	0	0	0	NC	4.75K
2GBytes	MIC2@	1	0	0	1	8.45K	2K
2GBytes	SAM2@	2	0	1	0	4.53K	2K
		3	0	1	1	6.98K	4.99K
4GBytes	HYN4@	4	1	0	0	4.53K	4.99K
4GBytes	MIC4@	5	1	0	1	3.24K	5.62K
4GBytes	SAM4@	6	1	1	0	3.4K	10K
		7	1	1	1	4.75K	NC

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.



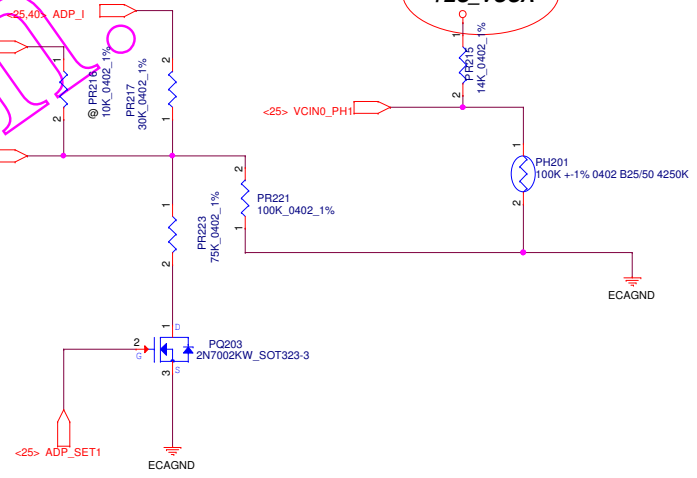
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Size	C	Document Number	LA-C281	Rev
Date:	Friday, February 06, 2015	Sheet	37	of 50



PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

Steve

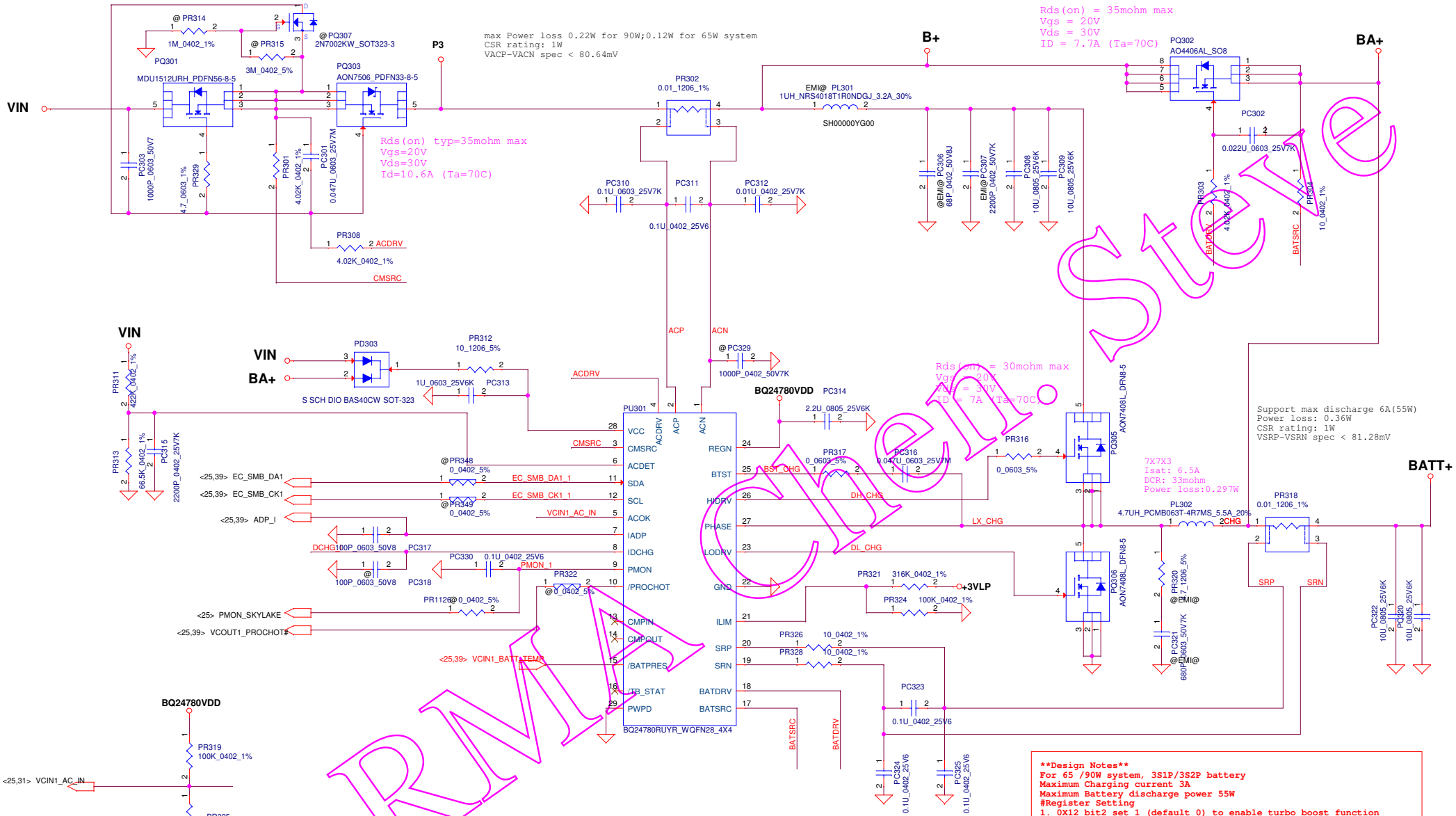
20120314
Change to +EC_VCCA from +3VLP



	ADP_SET1	ADP_SET2
45W adapter	0	0
65W adapter	1	0
90W adapter	0	1
135W adapter	1	1

135W: 150W active, 135W recovery
90W : 120W active, 90W recovery
65W : 85W active, 65W recovery
45W : 65W active, 45W recovery

For RMA



****Design Notes****
For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3A
Maximum Battery discharge power 55W
#Register Setting
1. 0X12 bit2 set 1 (default 0) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ILIM pull high voltage need base on 3/5V enable control
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W, L/S=1.2738W, Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. Charger timeout : No communication within 175s(default)
3. ACOCC : 3.33 X Input current DAC setting (default:Disable)
4. CHGOCP : based on charge current setting
5. BATOVF : 103-106%
6. BATLOWV : 2.6V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default:Disable)
9. IFAULT LOW : 230mV (default)

Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(316+100)/20/0.01
= 3.966 A

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				Date	Friday, February 06, 2015
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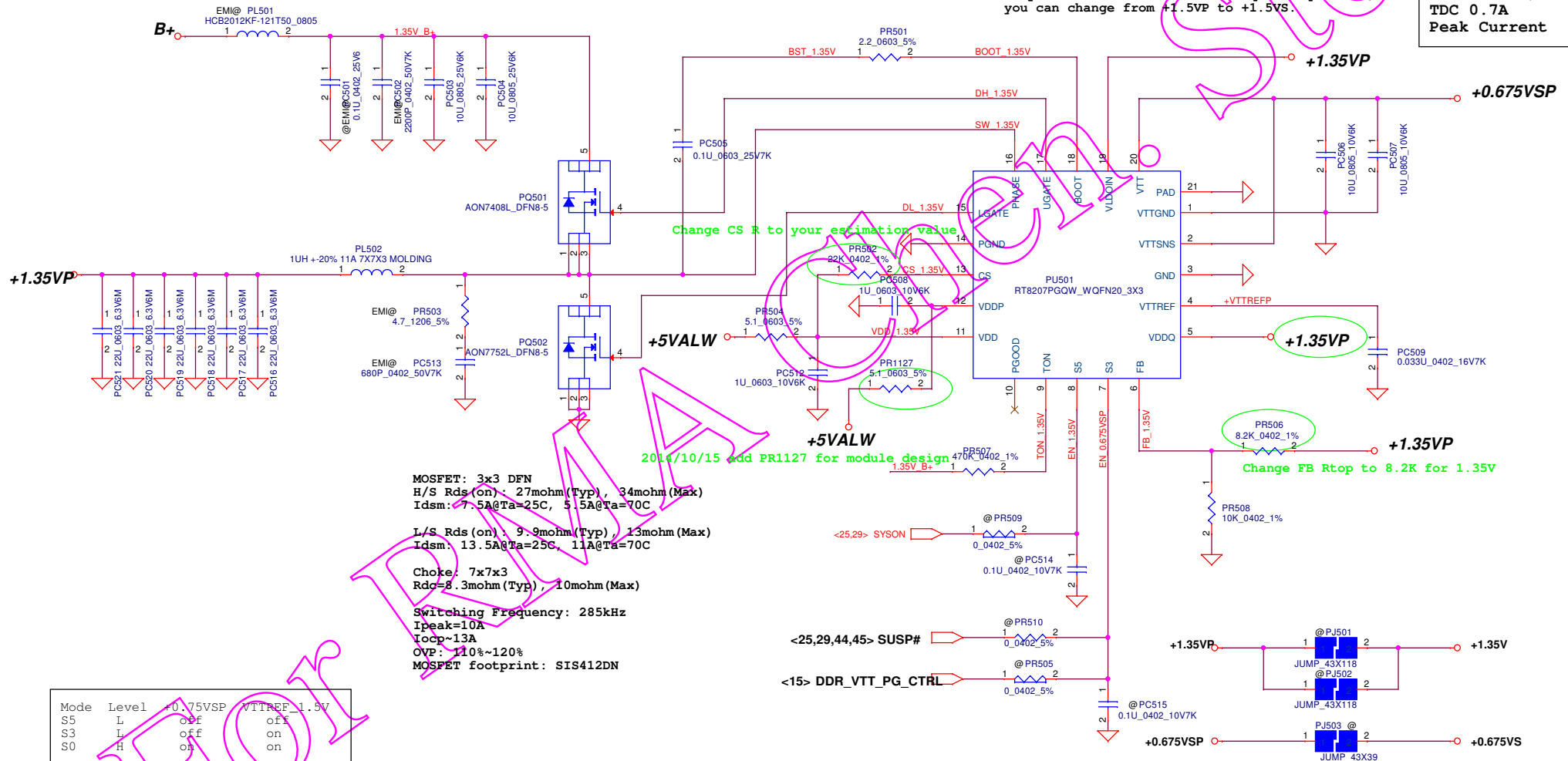


Module model information

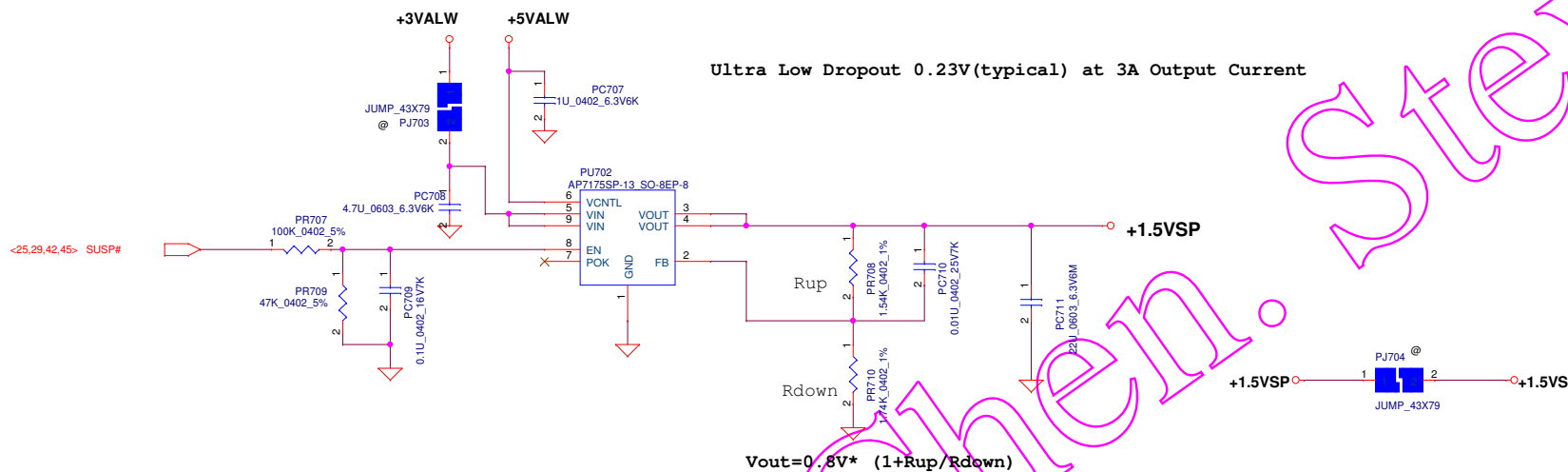
RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



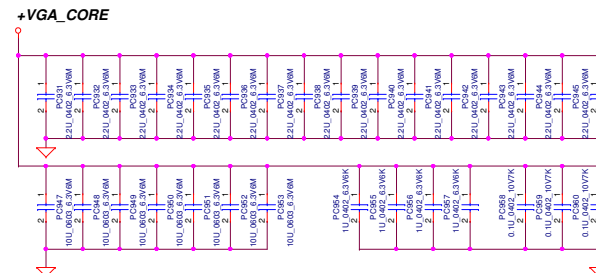
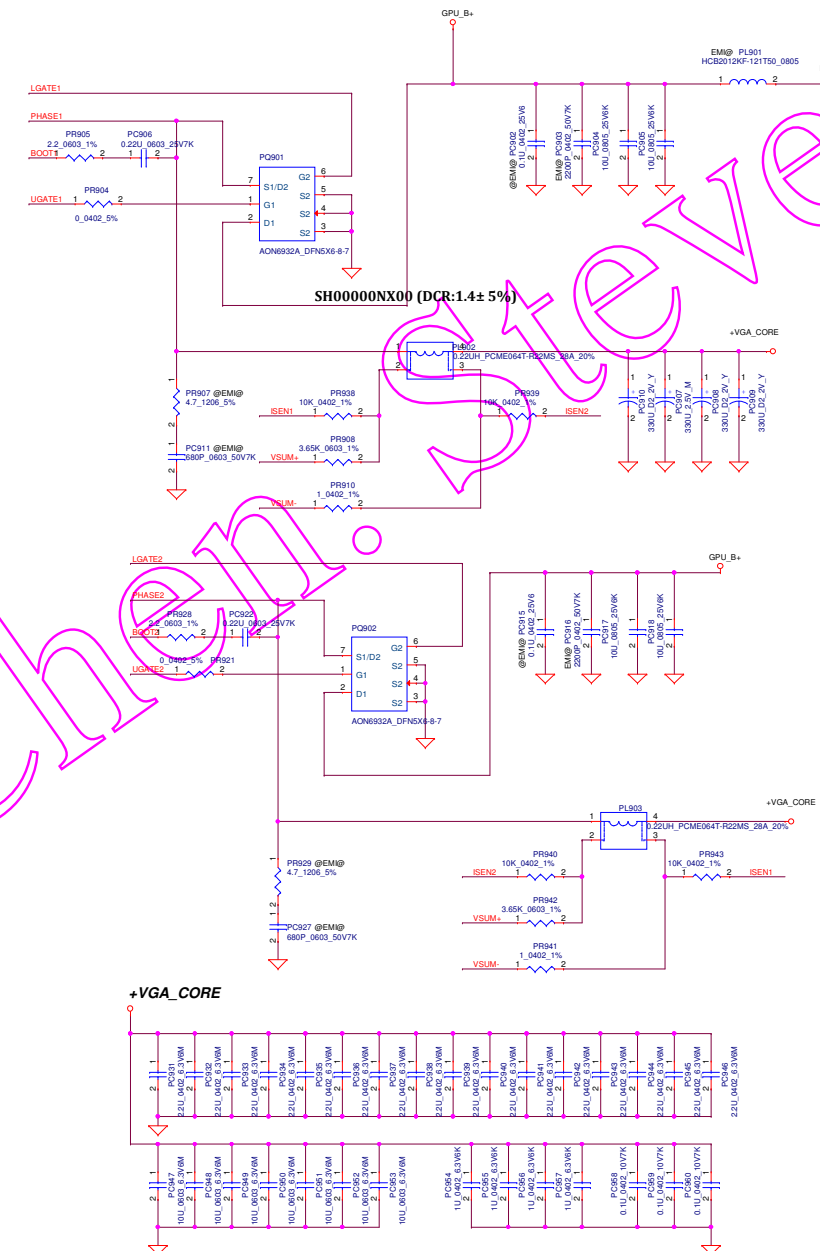
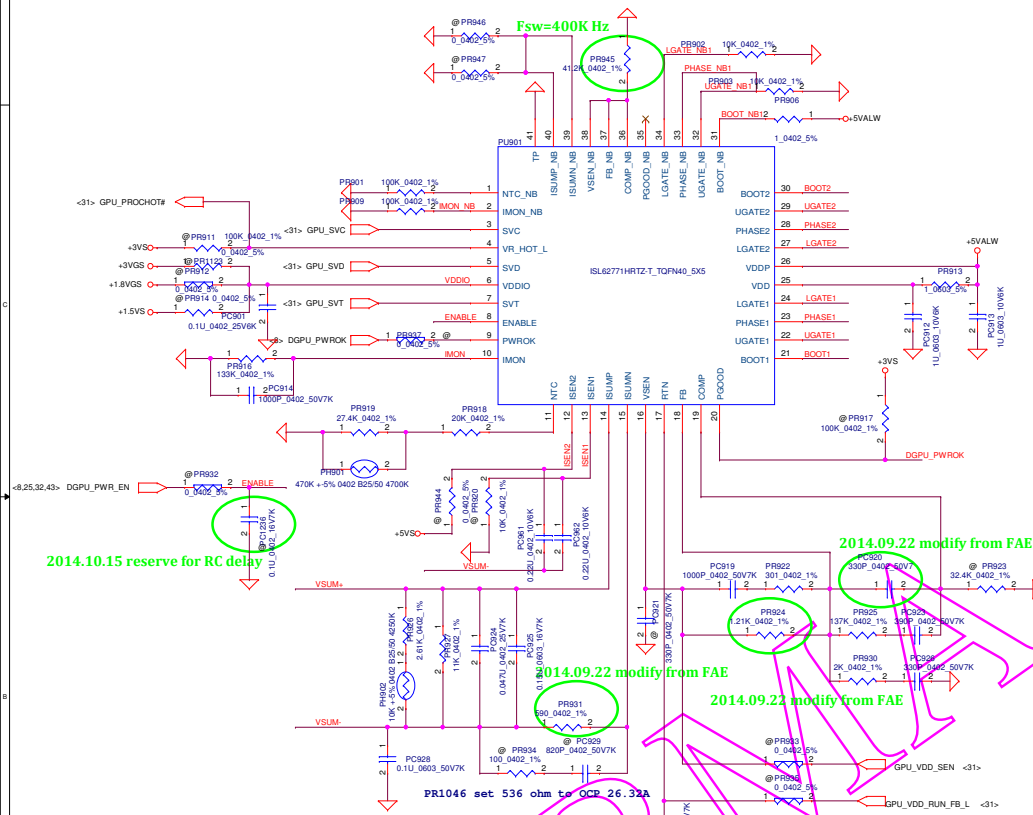
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Module model information
ISL62771_V1A.mdd for IC portion
ISL62771_V1B.mdd for SW portion

+VGA_CORE
AMD Meso XT
TDC 36A, EDC 54A
OCP min 67.8A



Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73

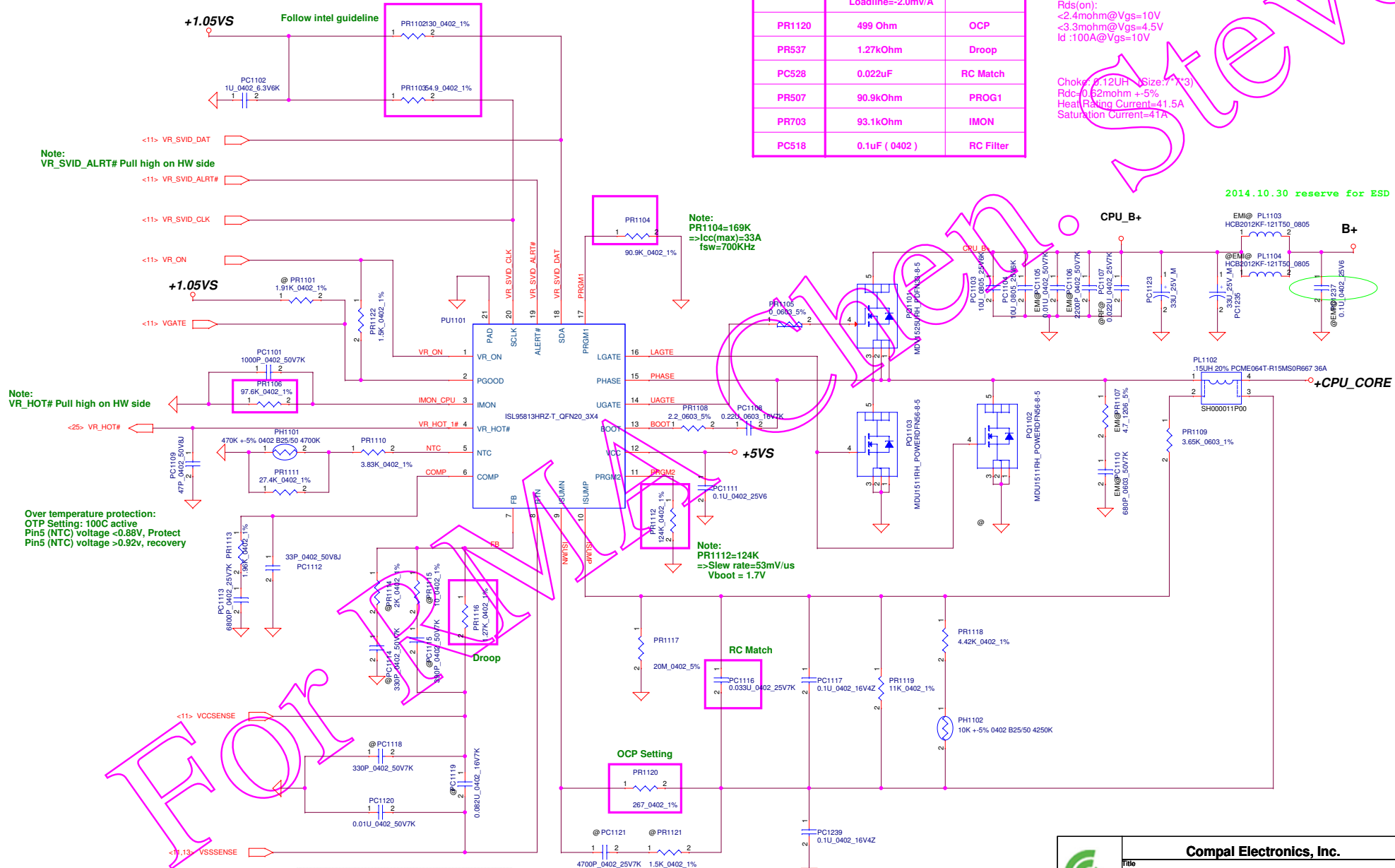
Location	15W	Note
	TDC 14A MAX 32A OCP 39A Loadline=-2.0mV/A	
PR1120	499 Ohm	OCP
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

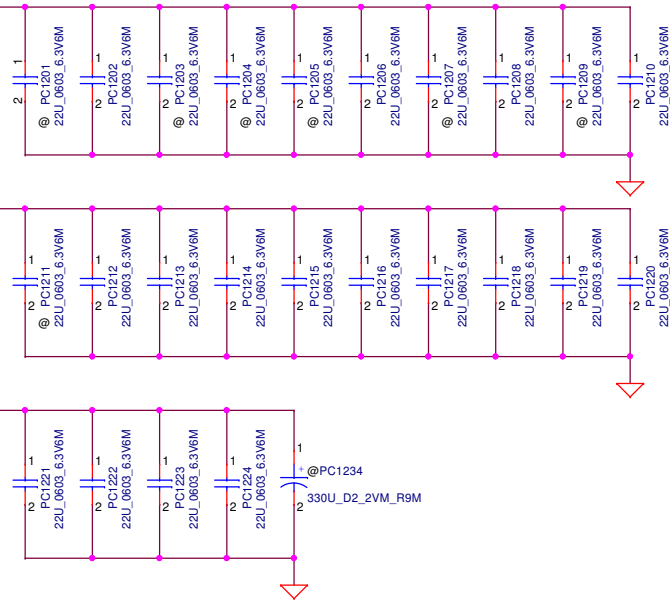
Choke: 0.12uH (Size: 7*7*3)
Rdc: 0.62mohm +5%
Heat Rising Current=1.5A
Saturation Current=41A

2014.10.30 reserve for ESD



+CPU_CORE

24 X 22u/0603



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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	reserve VGA_CORE RC delay	P46	add PC1236	2014.10.15	SIV
2	reserve 0.1uF for ESD	P41/P47	add PC1237,PC1238	2014.10.30	SIV
3					
4					
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				Document Number BE BDW	
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Version change list (P.I.R. List)			Page 1 of 1 for HW		
Item	Reason for change	PG#	Modify List		Phase
1	Reserve clean CMOS circuit	P06	reserve R80,Q27	2014.10.28	SIV
2	HDMI Design	P18	add R1650,R1651,R1652,R1653,R1654,R1655,R1656,R1657,R1658,R1659,R1660,R1661	2014.10.28	SIV
3	USB2.0 design for EMI request	P24	add R1676 and R1677	2014.10.28	SIV
4	Change commom chock symbol for EMI request	P24	change L12~L18	2014.10.28	SIV
5	Add FAN_ID for EC request	P25	add R516 and R517	2014.10.29	SIV
6	Audio design for EMI request	P36	add CA28,CA29,CA30,CA31	2014.10.29	SIV
7	Audio design for EMI request	P36	change from RA19,RA20 to LA2,LA3	2014.10.29	SIV
8	Audio design for EMI request	P36	add LA1	2014.10.29	SIV
9	+1.35V design for EMI request	P15	add C320~C324	2014.10.29	SIV
10	modify +MEM_GFX power sequence	P32	change C901 from 0.01uF to 0.1uF	2014.10.30	SIV
11	LAN design change for wake on lan	P26	delete RL18, add J6,J7	2014.11.13	SIT
12	Change pcb foot print by DFX request	P20,P24	change J101,JODD1,JHDMI pcb footprint	2014.12.08	SIT
13	Change for VGA power sequence	P32	change CV35 value	2014.12.08	SIT
14	Change Audio PCBEEP SCH by verdor suggestion	P27	add RA35,RA37,CA90,CA91,RA39 / DELETE CA23,CA24,RA36,RA34,CA25	2014.12.15	SIT
15	Modify LED BOM setting	P27	modify LED1,LED2,LED3,LED4,LED5,LED6 BOM setting	2014.12.15	SIT
16					
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